IMPLEMENTATION OF MICROCOMPUTER BASED CONTROLLER FOR HVDC SIMULATOR

A THESIS SUBMITTED

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Certificate

It is certified that the work contained in the thesis entitled " **IMPLEMENTATION OF MICROCOMPUTER BASED CONTROLLER FOR HVDC SIMULATOR.**", by **"VEKARIA MANOJKUMAR ZINABHAI"** , has been carried out under our supervision and that this work has not been submitted elsewhere for a degree.

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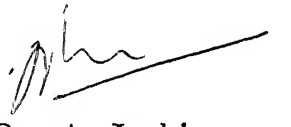

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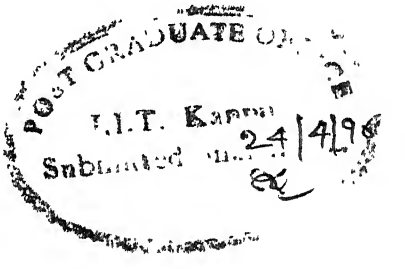

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ABSTRACT

A microcomputer based controller is designed in this thesis work for controlling HVDC simulator. All necessary interfacing cards to generate the required signals for implementation of microprocessor based digital control have been developed. The system is designed to operate from the serial port of a PC. The system is designed in the way so as to provide a very flexible, programmable platform on which HVDC simulations can be carried out and new converter control algorithms can be developed.

Dedicated

to

my Parents.

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List of abbriviations

A/D–Analog to Digital (converter).

AMV–Astable Multi-Vibrator.

CC–Constant Current.

CEA–Constant Extinction Angle.

CFA–Constant Firing Angle.

CT–Current Transformer.

DCCT–Direct Current–Current Transformer.

DIP–Dual In (Line) Package.

EMI–Electro-Magnetic Interferenace.

EOC–End Of Conversion.

EPC–Equidistance Pulse Control.

EPROM–Erasable Programmable Read Only Memory.

F/V–Frequency To Voltage (converter).

GTO–Gate Turn-Off (Thyristor).

IPC–Individual Phase Control.

LASCR–Light Activated Silicon Controlled Rectifier.

MCT–MOS Controlled Thyristor.

MMV–Monostable Multi-Vibrator.

MTDC–Multi-Terminal (HVDC) Configuration.

NMI–Non Maskable Interrupt.

PFC–Pulse Frequency Control.

PLL–Phase Locked Loop.

PPC–Pulse Phase Control.

RAM–Random Access (Read/Write) Memory.

RFI–Radio Frequency Interference.

SMPS–Switched Mode Power Supply.

SOC–Start Of Conversion.

USART–Universal Synchronous- Asynchronous Receiver- Transmitter.

VAR– Reactive Volt-Ampere.

VCO–Voltage Controlled oscillator.

VDCOL–Voltage Dependent Current Order Limit.

V/F–Voltage To Frequency (converter).

ZCD–Zero Crossing Detector.

List of symbols

α – Firing angle.

E_l – AC line to line Voltage (rms).

γ – Extinction angle.

γ_{ref} – Minimum extinction angle setting.

I_d – DC side current.

I_{ds} – DC side current referance setting.

R_c – Equivalent commutation resistance.

u – Overlap angle.

V_d – DC side voltage.

ω – Supply frequency (in radians).

Chapter 1

Introduction

1.1 General

In modern power systems, the HVDC systems are increasingly being used due to its superiority over HVAC systems in many respects. Its advantages of ability to transmit bulk power over long distances without stability concerns, ability to interconnect systems at different frequencies or systems belonging to different control zones, easy controllability of power exchange between systems linked by HVDC, power transmission over underground or underwater cable, ability to incorporate system stabilization measures etc. are the chief attractions to the system planners.

Over the years, the thyristor technology has improved a lot and higher and higher voltage and current ratings are becoming available. This, together with advances in digital electronics and availability of cheap microprocessor and related components has opened up a whole new scope for implementation of more complex and flexible control strategies for better integration of HVDC systems in the today's complex interconnected power systems network. Developments in gapless metal oxide surge arresters and fiber optics communication in HVDC bridge control has markedly improved the reliability of the HVDC stations. All these factors has led to the reduction in the cost of HVDC systems and hence reduction in the economic distance in comparison with HVAC transmission.

Continued developments on the technological front fuels the research efforts to tackle the problems posed by complex power systems network by developing better control and protection strategies for the overall system improvement. HVDC systems having such capabilities are thus one such area of extreme attention. Development of newer control

algorithms calls for extensive software simulations using different software tools. It is desirable that after satisfactory software simulation results, it can be tried out on a scaled down system for actual real time run of developed algorithms. This is the background for the present work.

1.2 Historical Background

In HVDC lab at IITK there is an HVDC simulator supplied by Robinson Electronic Instruments, England. The simulator consisted of two, 3-ϕ, 6-pulse bridge, connected back to back via two transmission line segments and smoothing reactors. The normal DC ratings of the simulator are 100 V and 1 A corresponding to 100 kV and 1 kA. The distributed transmission line is provided by two sections of lines each for 50 miles. Each section has 20 units of π sections for 2.5 mile of line. All units are provided with a switch to change the characteristics impedance between overhead line and cable. The converter on each end is six thyristor bridge and a bypass thyristor. It has manual and automatic control modes of operation. In manual mode, the firing angles are set at each end manually using a 3-ϕ synchro at each end. The automatic mode provides constant current-CC and constant extinction angle-CEA controls. It uses analog based predictive control for CEA. The fault simulation unit consisted of circuitry for applying faults like fail to fire, backfire, fire through faults on a given valve for the given duration along with scope triggering and monitoring circuits.

1.3 Motivation for the project work

The simulator used very old analog based design providing little flexibility for testing new control methodologies. With advances in digital electronics, redesign of the system was considered useful to provide a better flexibility and programmability for the HVDC simulator. To provide such an experimental platform is the aim of this work.

A microcomputer based system is designed herewith to be interconnected with existing power circuits of the physical HVDC simulator (scaled down HVDC system model) to replace the analog based controls. The system is designed to provide user interface through computer serial ports for ease of operation.

1.4 Thesis outline

The thesis is organised into five chapters begining with this introduction chapter. This is followed by second chapter which deals with preliminary background of the HVDC systems in general, with a view to outline the requirements of HVDC system and other design considerations to set the design objectives. The design objectives set are listed and based on that, a system is designed. The third chapter describes the hardware implementation details of the system designed herewith. Circuits on each of the cards are described one by one and then their interconnection details with the HVDC simulator are described. The fourth chapter deals with the software written for the controller card monitor/debugger, facilities available in monitor/debugger program, their commands syntax are described. Then description of one application program, that for implementing feedback type constant firing angle-CFA control is given. The last chapter, that of concluding remarks, gives some of the waveforms obtained with one application program that was executed on the system. The final section in this chapter gives some suggestions for carrying on further work both on hardware side and software side to enhance the utility of the system for experimentation. A bibliographic section at the end gives some of the references which are used in this thesis work. Appendix A-F gives some hardware oriented details important from the point of view of the actual user/program developer. Appendix-A list all the port address assignments and their functions. Appendix-B gives interrupt assignments and their use together with memory map. Appendix-C shows monitor/debugger commands syntax. Appendix-D lists all connector and PCB edge connector signals. Appendix-E contains complete circuit diagrams of all the four cards. Appendix-F gives component/connector layouts to locate any connector, trimming pots or any other components for all the five cards.

Chapter 2

Design Considerations

2.1 General HVDC systems

Basic HVDC system is a two terminal system consisting of a pair of rectifier and inverter stations. These stations may be interconnected through the length of a transmission line for long distance bulk power transmission or may be situated at the same place (back to back interconnection). The system may use unipolar, bipolar or homopolar configurations. Also the dc system may have a multi-terminal configuration (MTDC) consisting of interconnected network of more than two HVDC converter stations.

2.2 Components of HVDC systems

2.2.1 Rectifier and inverter stations

This is the most basic component of an HVDC system. Their function, as their names suggest, is to convert ac voltage to dc voltage in case ofa rectifier and vice versa in case of an inverter. They are collectively referred to as converters and in all practical circuits used for the purpose, can be made to function as either. Thus power flow direction over the line can be easily changed by reversing the roles of the converters at each end.

The most widely used basic circuit for the converters is 3-ϕ, 6 pulse bridge circuit. This choice is arrived at by almost universal use of 3-ϕ ac system for power transmission world wide and 3-ϕ, 6 pulse bridge has best figures of transformer and valve utilization factors. However in all practical systems, two such bridges, each fed from a supply differing by

30° which are easily provided by Y–Δ and Y–Y connected transformers, are connected in series to get effectively 12 pulse configuration. This reduces dc side ripple as well as ac side current ripples which reduces filtering requirements by the elimination of 5^{th} and 7^{th} harmonics on ac side and 6^{th} harmonic on dc side. Higher pulse no.s are not used due problems in getting proper supply for them in view of supply voltage unbalances which, together with firing imbalances produces non-characteristics harmonics.

2.2.2 Bridge elements

In all modern designs, the thyristor has replaced mercury arc valves due to availability of higher voltage and current ratings due to advances in semiconductor technology and better cooling methods employed. This has reduced the cost of providing for overload capabilities and also allows lower converter transformer leakage reactances and thus, in turn, improves the power factor. Also availability of Zn oxide gapless surge arresters has reduced the cost of providing over voltage protection to the thyristors and has improved reliability of the thyristor converters. Recent advances in GTO, MCT, LASCR technologies are also promising for the future. Till these technologies mature, the thyristors are here for use in the HVDC converters. As power levels encountered in the HVDC systems are very high, the voltages up to 500 kV and current levels of 2 kA are also not uncommon. To handle this high levels of voltages and currents, each element of the bridge arm consists of no. of series and parallel combinations of the thyristors. This calls for careful design of the string for proper voltage and current sharing both for static and dynamic changes so that equal sharing is ensured and hence lower safety margins to be provided.

2.2.3 Converter transformers

Converter transformers are needed for matching the voltage levels of ac supply side and desired dc side voltage levels. The 12 pulse converter requires two 3-ϕ supplies differing by 30°. This is provided by Y–Y and Y–Δ transformer connections. The transformer itself may consist of a bank of 1-ϕ transformers or one or two 3-ϕ transformers. The transformer leakage reactance has to be chosen with due regards to limiting the short-circuit currents through the valves during overlap durations and other fault conditions. Due to imbalances in the firing, which may result in dc magnetization of the core, the magnetic circuit has to be properly designed with appropriate air gaps to avoid core saturation. A tertiary

Δ–connected winding may be used to provide a path for third harmonic currents and for connection of filter and reactive power compensation circuits.

2.2.4 Smoothing reactors

A large air core reactor is used on dc side to smoothen dc current and also to limit the rate of rise of short circuit current in case of line faults. It is inserted at both terminals either at line end, neutral end or midway position.

2.2.5 Filters

Due to nature of current waveform taken from ac supply, which is very rich with np$\pm$1 harmonics, it is imperative to use harmonic filters on ac side. This provides low impedance shunt paths for harmonic currents and hence prevents them from entering the supply grid. Also high frequency filters are also inserted between converter station and both ac and dc lines to prevent RFI/EMI interference to other services. Harmonic filters also serves additional purpose of supplying the reactive power drawn by the converters.

2.2.6 Reactive power source

Each converter station draws large amount of reactive power depending upon the active power being transmitted and firing angle used. An automatic on load tap changer can help to keep reactive power requirements of the converters to minimum. Rest has to be taken care of by external means like switched shunt capacitors, synchronous condensers, static VAR systems etc. As was mentioned, filters contribute to this requirement by being capacitive at power frequency.

2.3 Bridge circuit operation

The analysis of bridge circuit is carried out assuming dc current to be constant. This, in HVDC systems which uses large reactors on dc side, is justified in steady state for current levels above certain minimum value. The firing pulses to HVDC bridge is generally continuous signal of 120^o duration to ensure firing of thyristors even under worst conditions. So even if some transient reduces current through the thyristor below holding current, it

can again start conduction with resumption of favorable conditions. With source reactance taken into consideration, the commutation from one valve to another valve takes finite time and thus, there is an overlap period during which more than two valves conduct. With this overlap duration less than 60°, the converter operates in 2 and 3 valve conduction mode. For operation in this mode, the following relations can be derived.

$$V_d = \frac{3\sqrt{2}}{\pi} E_l \cos\alpha - R_c I_d \tag{2.1}$$

$$V_d = \frac{3\sqrt{2}}{2\pi} E_l (\cos\alpha + \cos(\alpha + u)) \tag{2.2}$$

$$V_d = \frac{3\sqrt{2}}{\pi} E_l \cos\gamma - R_c I_d \tag{2.3}$$

$$I_d = I_s(\cos\alpha - \cos(\alpha + u)) \tag{2.4}$$

$$I_s = \frac{\sqrt{2}E_l}{2\omega L} \tag{2.5}$$

2.4 Firing angle controls

The two methods of firing angle control are individual phase control-IPC and equidistant pulse control-EPC. In the former case, firing angles are generated individually with reference to their commutation voltages, while in the later case, only single commutation voltage acts as a reference for firing corresponding valve and all other valve firings are at 60° interval to the previous firing. This way, equidistance is ensured in firing in steady state. The IPC control is nowhere in use due to its tendency to generate non-characteristic harmonics which are very difficult to filter and may lead to harmonic instability even though the performance of IPC is better for unbalanced voltages than EPC which gives higher negative damping to torsional oscillations. Equidistance firing signals can be generated by both analog and digital means. There are variations like pulse frequency control-PFC, pulse period control-PPC both of which has integral characteristics with former having error averaging in-built when generated by analog means using a VCO. Another method namely pulse phase control has advantage of easily incorporating angle limits and also easy linearisation of CC controller by providing inverse cosine block. When implemented using μP in conjunction with analog signal processing, any of the above schemes can easily be incorporated. It will provide much more flexibility in firing angle generation and control implementation.

2.5 Converter controls

The salient points important from the view point of converter controls are described herewith briefly.

Although the basic function of the HVDC systems is transfer of desired amount of power from one station to the other, feedback control of power is not desirable due to high current levels required at low voltages causes excessive reactive power demand and thus, tends to reduce the already low levels of voltage. Also constant power characteristics leads to negative damping and degrades dynamic stability.

Usually, the power flow over the line is varied by adjusting current levels to required values keeping voltage at its near maximum value. This ensures lower line losses, lower reactive power demand and optimal utilization of insulation provided.

Under normal conditions, the rectifier is assigned for current control. This has advantages that higher power levels demand reduction in firing angle at rectifier end and hence reduces its reactive power demand. Exactly the reverse is the case with current control at inverter end. Current control at rectifier end also limits the line fault current automatically. And by allowing operation at minimum extinction angle γ at the inverter end also reduces its reactive power demand.

While it is advisable from point of view of reducing reactive power demand at inverter end to keep γ at minimum value, some minimum value has to be kept to prevent commutation failures. Since γ is not control variable directly, some predictive or feedback or combinative technique is used when minimum constant extinction angle control-CEA is used.

At rectifier end, the on load tap changer is operated such that firing angle remains in the range $10°$–$20°$ to limit the reactive power demand. Here too, as low value as possible for firing angle is desirable, but to provide for regulation of current, some movement margin has to be allowed as tap changer control is too slow. Also minimum α limit is also placed at $5°$–$8°$ to ensure that all the valves in the series connected string has some minimum forward voltage before firing pulse appears.

As we have seen, rectifier is operated in constant current-CC control and inverter in constant extinction angle-CEA control normally. But when rectifier end voltage reduces, the only way to maintain power flow is by operating rectifier end at minimum alpha and assigning the current control to the inverter end. Thus, in addition to providing CEA

control at inverter end, CC control is also provided and to avoid both CC operating simultaneously, the reference value for CC controller at inverter end is made lower. So only when the rectifier CC controller fails to keep current value above the reference setting of current for inverter end CC controller, inverter end CC controller takes over. Usually reference value at inverter end is kept 10 % below the reference current value at rectifier end.

As the converter can function both as a rectifier as well as an inverter, the power reversal on the line can easily be affected by providing both controls at both the ends. Relative values of reference current setting for CC controller at each end decides the power flow direction. By making the reference value of current setting at inverter end higher than that at rectifier end causes power flow direction to change from inverter end to rectifier end. This can be prevented by limiting the control action only to one mode of operation, either rectification or inversion, if so desired.

The basic control characteristics as depicted in Figure 2.1 can be modified suitably to eliminate 3 point instability, commutation failures at reduced voltages etc. VDCOL is one such scheme where characteristics are modified to as shown in Figure 2.2.

The CC controller is usually feedback type PI controller. As the gain of the system is non-linear cosine function, an inverse cosine block may be included in the feedback control loop to linearise it for near uniform response throughout the control range.

Constant extinction angle control may use feedback or predictive or combination of both for the control implementation.

2.6 Control hierarchy

The master controller for a given HVDC system receives power order settings from energy control center of the region which monitors the status of the power system and depending upon the generation availability, load demand, agreed power exchange between the regions and other factors, decides the desired power flow levels over the given HVDC system. This then are transferred to the master controller for the given HVDC system which, in turn, calculates the reference current settings for each converter stations and transfers them to respective terminals of HVDC system by means of high speed communication links.

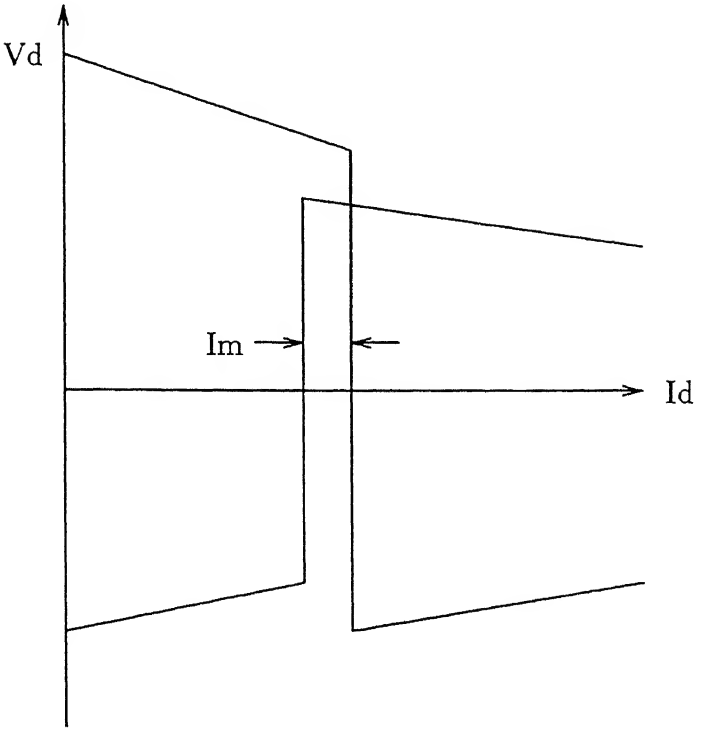

Figure 2.1: Basic control characteristics of HVDC bridge.

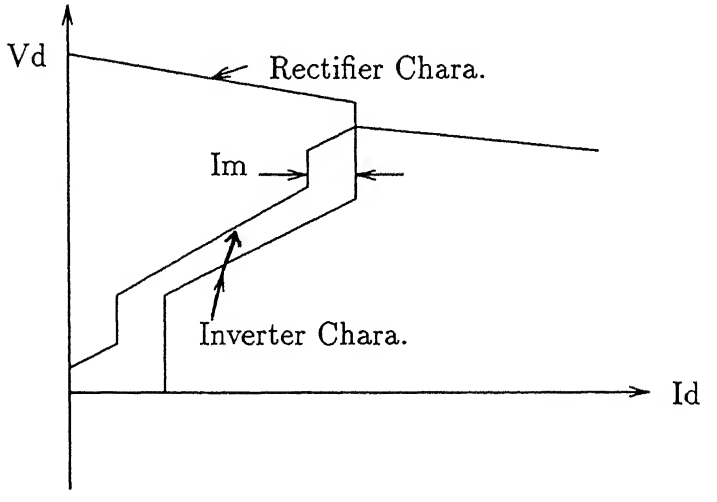

Figure 2.2: Modified current order limit control-VDCOL.

2.7 Auxiliary controls

In addition to normal function of transmitting power, HVDC systems may be called on for other auxiliary functions for ac system improvement. These functions may be damping of low frequency inter area power oscillations by power modulation over interconnecting HVDC lines, sub synchronous damping controls, reactive power controls, including power–frequency control to make dc power flow frequency sensitive and other emergency controls.

2.8 Design objectives

With the aim of providing a good, flexible hardware platform on which HVDC system control and simulation experiments can be carried out, following design objectives were set keeping in mind the given constraints.

- Easy interface to the user through use of computer.
- Compatibility with the existing HVDC simulator hardware.
- Features of the existing hardware to be preserved as far as possible with minimum changes to be made in the existing set up.
- μP based controller design to provide flexibility and programmability.
- Ease of program development, faster program evolution/refinement/testing of new control algorithms and simulations.
- Timing measurements of angle to be made with precision of 0.1^{o}.
- Hardware options for fault initiation and its synchronization with other internal or external events in addition to software fault simulation options.
- Analog signal inputs through A/D channels for control, protection, monitoring or data logging purposes.
- Options of PLL based clock or crystal clock for timing measurements
- Clear modular design for ease of operation, maintenance, trouble shooting and further upgradations/alterations.

2.9 Existing hardware

2.9.1 Converter unit

Converter unit consists of 3-ϕ, 6 pulse bridge circuit rated for 100 V, 1 A. Thyristors are used as bridge elements with ample over current and over voltage capabilities. An RC circuit is connected across each of the thyristors to damp oscillations at beginning and end of the commutation. A seventh thyristor is connected across the dc output as a bypass valve. When a fault is detected, the firing pulses to all valves are blocked and the bypass valve is fired which short circuits the dc side. The bridge is fed from three, 1-ϕ transformers having three windings each. The primaries of three power transformer are connected in Y with 4-wire connection. The secondaries may be connected in Y or Δ by a manual, off-load switch which also changes connections of three other auxiliary transformers which produces six commutation voltages. The third winding on the power transformers are connected in Δ to act as a tertiary winding to circulate the third harmonics currents. They may also be used for connection with external filter networks. The primary winding has on-load tap changer with tap range of 0.9 – 1.15 in steps of 0.05 p.u.

Three current transformers with ratio 100:1 are connected in each line between secondary of converter transformer and bridge. The outputs of these CT's are rectified by a diode bridge and fed to 500 Ω load resistance. The voltage developed across it is used for protection purposes.

Each of the main thyristors are fired by a pulse transformer capable of sustaining continuous pulse firing which is used here. This period may extend up to 240° under transient conditions. The bypass valve may be required to conduct for much longer durations. To provide continuous firing for this long duration, two pulse transformers, each fed from a square wave signal is used. Both signal are at 180° phase difference with slight overlap duration for direction corresponding to firing. This two signals are rectified and combined at the output to give continuous firing signal for the bypass valve.

There is one dc current transformer in common anode pole of the bridge with ratio of 100:1, the secondary of which flows through 500 Ω resistance and the voltage obtained across it is used in the protection circuit and also for CEA control circuits.

There is one reactor provided at each end which can be inserted in either anode or cathode side. There is an RC damping circuit across it to damp oscillations. There is one

secondary wound with a ratio of 50:1 to obtain rate of change in dc current signal which can be used in control or protection circuits.

2.9.2 Line unit

The line unit consists of single pole π sections of simulated line segments. Total 50 such sections are provided, each representing 2.5 mile of line totaling 50 miles. The characteristic impedance can be changed between overhead line and cable, by toggling the switch provided in each section.

2.9.3 Manual control unit

Three phase commutating voltages obtained from auxiliary mains step down transformers are fed to three phase synchro when manual mode is selected. With slow motion drive, the rotor position of the synchro can be adjusted to any position 0–360° shifting the three phase output of the synchro by same amount. The output of the synchro is fed to three center tapped secondary transformers to provide six phase shifted voltages. This six outputs are loaded with an RC circuit formed by a potentiometer and a 2 μF capacitor to null any phase shift inaccuracies. In manual control mode, this six signals are applied to six pulse circuits whereas in automatic mode, pulse circuits receives signals from automatic control unit.

The pulse circuits are designed for starting firing pulse when ac input voltage crosses zero while going positive and stops it when next valve in the same group is fired similarly. The pulses can be blocked by applying 4 V to pulse blocking input.

2.9.4 Automatic control unit

2.9.4.1 CEA control

There is one constant extinction angle-CEA control circuit for each of the bridge elements. The CEA control is based on the integration of commutation voltages for correct prediction of the valve extinction instants on the lines of scheme proposed by Hingorani and Chadwick[1]. An op amp integrator is used to integrate the commutation voltage for the corresponding valve from period $(-\pi + \gamma_{ref})$ in every cycle from zero reset value. The output of this integrator is added with $2\omega \mathrm{LI}_d$ signal obtained by proper setting of

potentiometer on DCCT output. The overall signal is sent to pulse circuit for firing pulse generation.

2.9.4.2 Constant current control

Only one constant current control circuit is used on each side. The range of CEA control circuit can be extended by further adding V_{cc} signal at the summing junction. The V_{cc} signal is obtained by constant current control. This is done by integrating difference signal of DCCT output signal and current setting signal I_{ds} set using pot. The difference signal is amplified only when $I_d < I_{ds}$. For $I_d > I_{ds}$ the converter operates on CEA control else on CC control. There is a risk of making V_{cc} too large and hence summation signal may not go negative at all and thus pulse circuit will fail to operate. This can be avoided by adding a negative going pulse of sufficient amplitude at positive zero crossing of the commutation voltage.

2.9.4.3 Transient ac voltage control

Sudden changes in supply voltages can lead to commutation failures. If such changes are detected early enough, then correction can be applied in the firing signal to avoid commutation failures. This circuitry is implemented here, by adding a fraction K of commutation signal and integrator output. This combination signal passes positive zero crossing at $\omega t=90^\circ$ for small values of γ_{ref} and unity K. By changing fraction K from unity to zero changes the instant when this signal passes positive zero crossing from 90° to $(180^\circ-\gamma_{ref})$. The fraction K can be chosen to cover maximum part of the cycle and be sufficiently advanced for any compensation to be applied. This value is set to proper value using a potentiometer provided for the purpose. Any sudden rise in the ac voltage will cause the advancing of the zero crossing instant of combined signal. This condition is sensed to provide compensation in next firing.

2.9.5 Protection unit

The overcurrent sensing circuit operates using signal from DCCT and has two sections, for sensing fast rise in the current and for sensing slow rise in current above certain fixed value. The backfire detector circuit operates using difference signals of DCCT and ac CT's. Backfire is equivalent to ac short circuit and hence ac current increases but dc

current does not increase and hence, net negative signal is available. The commutation failure is equivalent to dc short circuit and hence dc current increases but ac current do not increase and hence net positive signal is available. Two circuits, one operating on positive going signal and the other operating on negative going signal with some threshold fixed on each side is used for detecting respective fault conditions. Other circuits contained in this unit are unsustained blocking and duration setting circuits, main blocking circuits, bypass continuous pulse generator circuits and reset circuits.

2.9.6 Fault simulation unit

This unit contains circuits for fault type selection from fail to fire, fire through and back fire, valve selection for fault to be applied, its duration and delay settings and some oscilloscope triggering and monitoring circuits. The user settings are appropriately interpreted and necessary follow up action is initiated.

2.10 Proposed system

After considering all the aspects of the HVDC systems in respect of control and simulation requirements, together with earlier set design objectives to be met with given constraints, a μP based system with following features was decided.

The interface provided to the user is through a computer, a PC in this case equipped with RS232C ports. This PC is linked by two RS232C serial links to each of the converter stations. The PC may emulate the functions of energy dispatch center in broad operational matters like deciding upon the power transfer levels. It also has to act as an operational console where the user can set all the system operational parameters, monitor the system status, set different fault simulation commands and observe its impacts. Also new bridge control algorithms developed can be loaded through the serial links for subsequent execution.

In addition to the serial links with PC, each of the converter ends are interconnected through an additional dedicated serial link so that each terminal can exchange information directly without resorting to routing it through PC in view of enhanced speed and leaving PC to do other tasks.

Converter at both the ends has a separate μP based controller card to take care of all

operational aspects of each of the converters. This card provides the two serial links that link central PC and other converter station as was mentioned in the previous paragraph. The EPROM resident program of these cards is a full feature debugger similar to the 8086 based μP kits having facilities to be used from PC serial port. This program can load user programs from PC to controller card for subsequent execution and debugging with facilities for single stepping and execution with break points etc. for ease of program developmental work. Satisfactorily working user program may also be put in resident EPROM memory for direct execution without needing loading every time.

The controller card also incorporates other peripheral circuits for port control, interrupt handling, memory, counter, crystal time base, interfacing circuits for other cards etc.

The basic signals needed for any implementations of μP based control of HVDC bridge are: voltage zero crossing instants, valve current extinction instants, DC current value for CC control, timers for generating desired firing delay etc. All of this signals are obtained by a set of interfacing cards.

The interfacing card for firing signals has facilities for applying forced ON–OFF signals manually or through external hardware that can be designed according to user's experimental needs to apply it in synchronism with external events. This is in addition to the same facilities that can be provided through software. It has provisions for continuous firing, both modulated and unmodulated, with internal or external modulating signals, with instant turn-on even at low modulating frequency. It can also be configured for pulse firing though it is not the mode in which HVDC bridges are operated. It also has hardware blocking and bypass signal inputs. Firing signals are passed through one more level of isolation using optoisolators to effectively decouple power side transients from entering control circuitry. The 8 bit port on this card receives firing signals from controller card.

The interfacing card for zero crossing signals and other analog circuits uses six zero crossing detectors for giving interrupts at positive zero crossing of each of the six commutation voltages with individual threshold setting and in-built hysteresis for noisé free operation. Each of the three phase voltages are rectified using precision fullwave rectifier circuit and are available on three lower channels of 8 channel analog multiplexer. A very fast, 12-bit, A/D converter on board is used for interfacing analog signals to μP card. The five free channels of the 8 channel analog multiplexer are not used and are available to the user. A PLL is provided on board to generate clock at 3600 times supply frequency.

So each pulse of it corresponds to 0.1° and hence all timing measurements can be made using this clock frequency irrespective of supply frequency variations, with a precision of 0.1°. Alternative clock frequency of 1 MHz is also available for this purpose by changing analog 2-way switch position through software. Interface to controller card is through four, 8 bit ports. Two of them are used for 12-bit A/D converter outputs, one for voltage status reading and one for analog multiplexer settings.

The third interfacing card consists of circuits for getting valve current extinction instant sensing. Here the signals are derived by putting a small 1 Ω resistance in series with each of the bridge arms or in bridge supply leads. This signal is given to zero crossing detector circuits which, in turn, drives opto-isolators as all of this signals are at line potentials and needs to be kept well isolated from rest of the circuitry. This also calls for isolated supplies to drives each of the sensing circuits in all three phases. An SMPS is provided on board for this purpose for generating eight isolated ±15 V, 100 mA supplies from +15 V input. The present card uses four of these supplies for circuits on the card and rest of the four are available for other uses. The fourth supply is used for V/F converter circuits used for DC current and DC voltage inputs. As dc voltage and current signals are also at the line potential and in view of difficulties in sensing them with isolation, this scheme is used. Two V/F converters with linearity of the order of 0.03 % and full scale range of 0 to –10 V, 10 Hz–10 kHz are driven from an isolated supply. The input signals to V/F converters is voltage and current signals sensed by voltage divider and current shunt at a common junction. The output of the V/F converter is frequency signal which is isolated by opto-isolators. The output of the opto-isolators is directly used to generate interrupt signals. Back conversion to voltage by F/V converter was reducing the speed of response drastically due to use of filters. So to keep very high speed of response of V/F converters intact, necessary back conversion is done in the software or modifying the controller to take this signal as control variable. The interface to the controller card is through two ports which are used for inputting valve ON–OFF status and for identifying valve that caused current extinction interrupt. As this card contains interfacing circuits with live connections, it has to be handled with proper care when in ON condition for the safety of the operating personnel.

Chapter 3

Hardware description

3.1 Hardware organization

The overall block diagram of the system is shown in Figure 3.1. The functional block diagram of the HVDC simulator controller on one side is as shown in Figure 3.2. The complete circuitry for the project work is divided on five different cards according to their functional aspects. Four cards contain all the needed circuitry and the fifth one serves as a mother board containing all the interconnections. The cards and the mother board are designed for 19" standard rack mounting. Provision is made on the mother board for addition of one more card in case some expansion of hardware circuit is planned afterwards. The four cards that plug into the motherboard are :

- Card1: Firing signal interface card containing firing signal modulation, blocking and isolation circuits.
- Card2: Controller card containing 8086 μP based system with peripherals.
- Card3: Analog signal processing card containing circuits for voltage zero crossing detectors, 8 channel 12-bit A/D converter, PLL and voltage status ports.
- Card4: Live signals interface card containing valve extinction sensing circuits, V/F converters for dc current and voltage sensing, SMPS etc.

We will start describing the circuits on different cards one by one starting with controller card that is central to the functioning of the system. After describing the functions performed by four cards, we will describe their interconnections which are provided by the

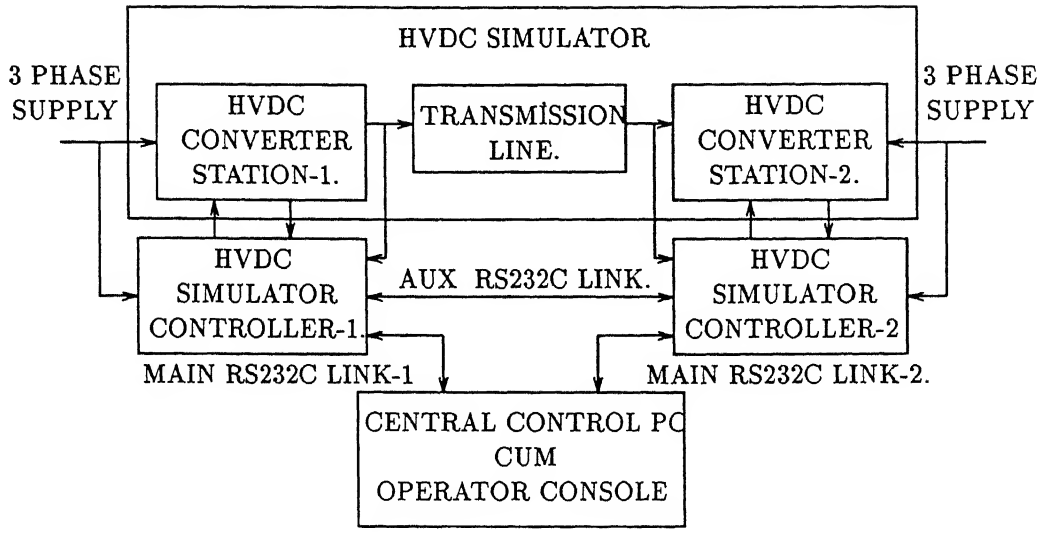

Figure 3.1: Overall system block diagram.

motherboard. Finally we will describe the interconnections of the whole system with the HVDC simulator. The functional aspects of the circuits are being described rather than the minute implementation details, which would have become elaborate. The complete circuit diagrams are given in Appendix-E which may be referred as and when required. The system bus structure is as shown Figure 3.3.

3.2 Controller card circuits

From the point of the view of ease of availability, software support, speed and cost considerations, 8086 based design was chosen. Block diagram of the circuits on the card is shown in Figure 3.4.

The system clock is derived from 14.75 MHz crystal which also serves as a clock for baud-rate generator for on-board serial link interfaces. An 8284A clock generator divides this frequency by 3 to generate system clock frequency of 4.9 MHz which would provide adequate speed for the present application. A wait state generator circuit adds one wait state for each I/O operation. As the memory chips are fast enough, they do not need wait states. The 16-bit data bus and 20-bit address bus is separated and buffered by two 74LS245's and three 74LS373's. The system memory requirements are met by two 27C256 EPROMs (256k $\times$ 16-bit) and two 65256 RAMs (256k $\times$ 16-bit) which would

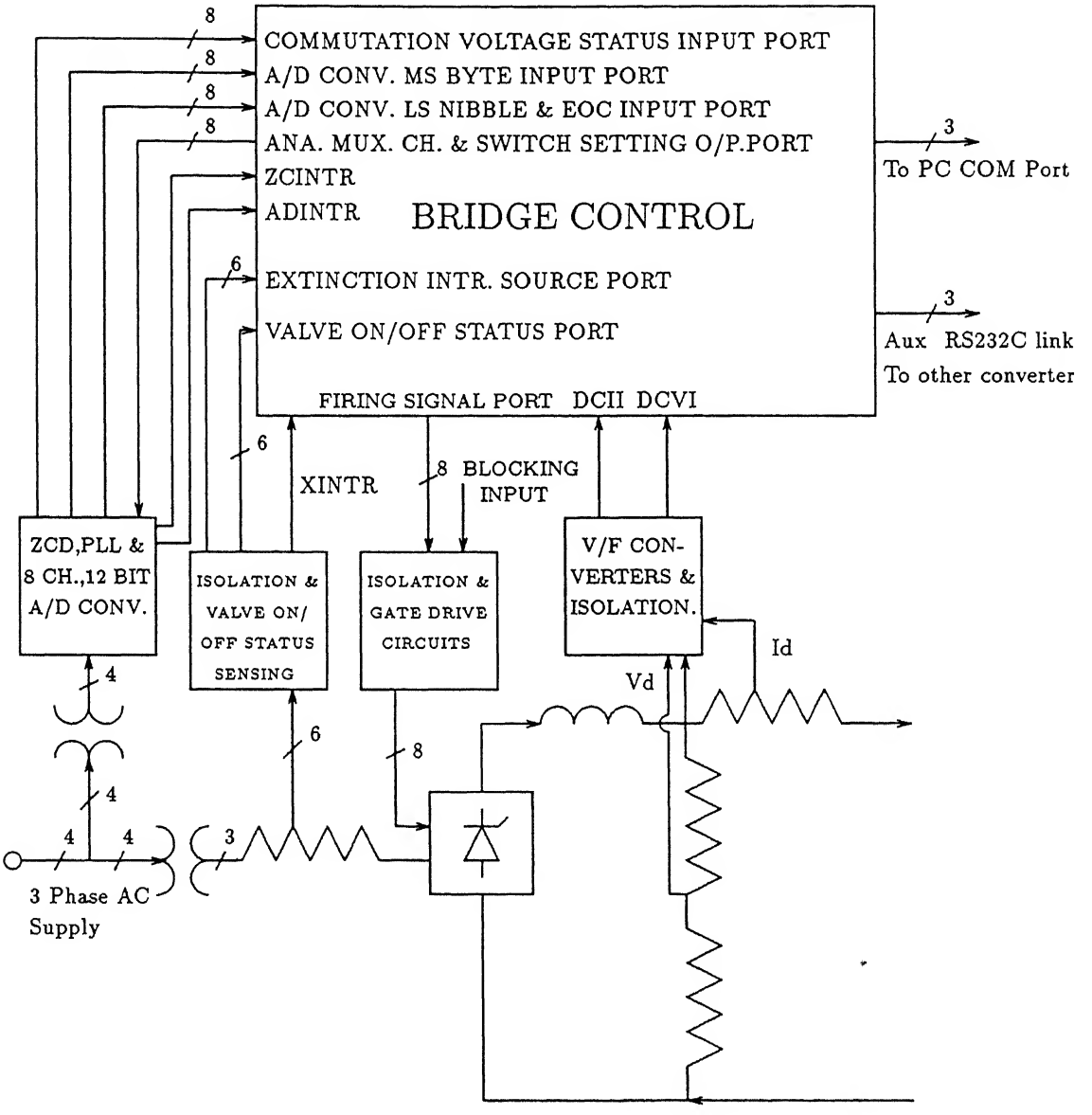

Figure 3.2: Functional block diagram of HVDC simulator controller.

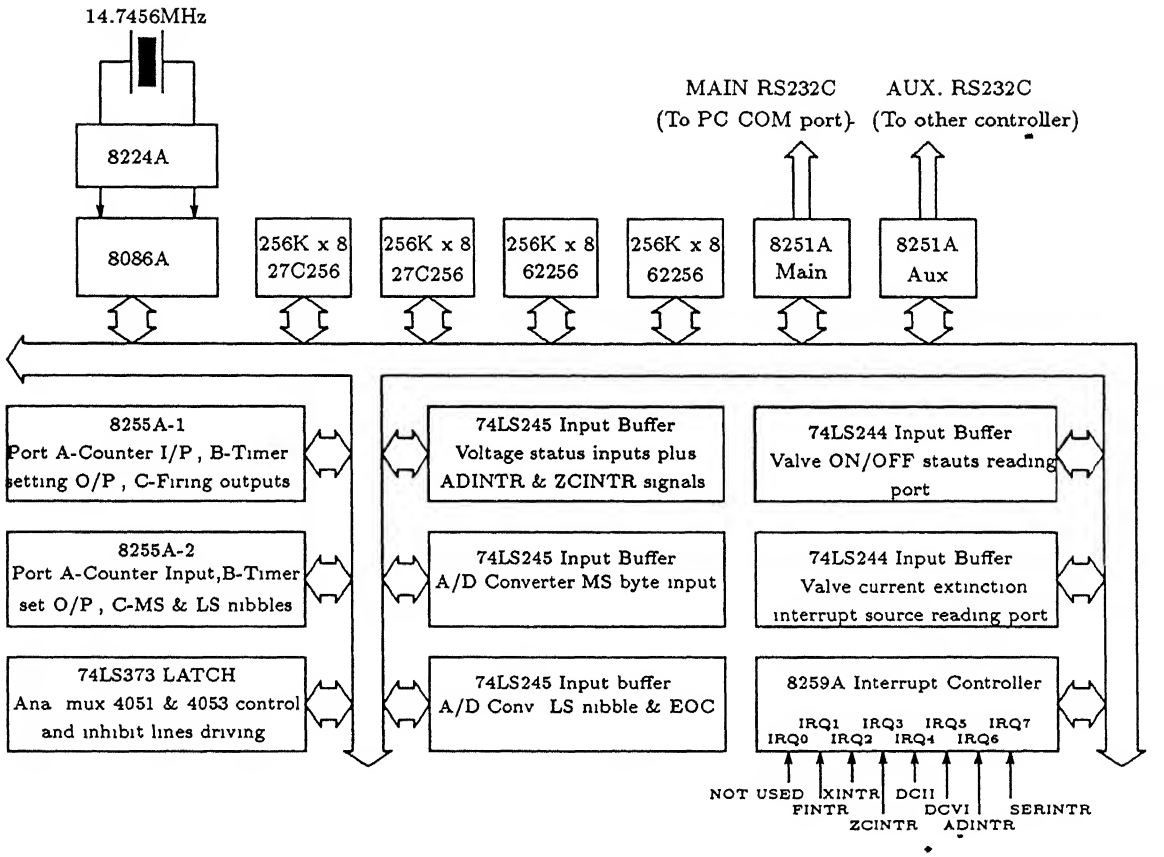

Figure 3.3: System bus connections.

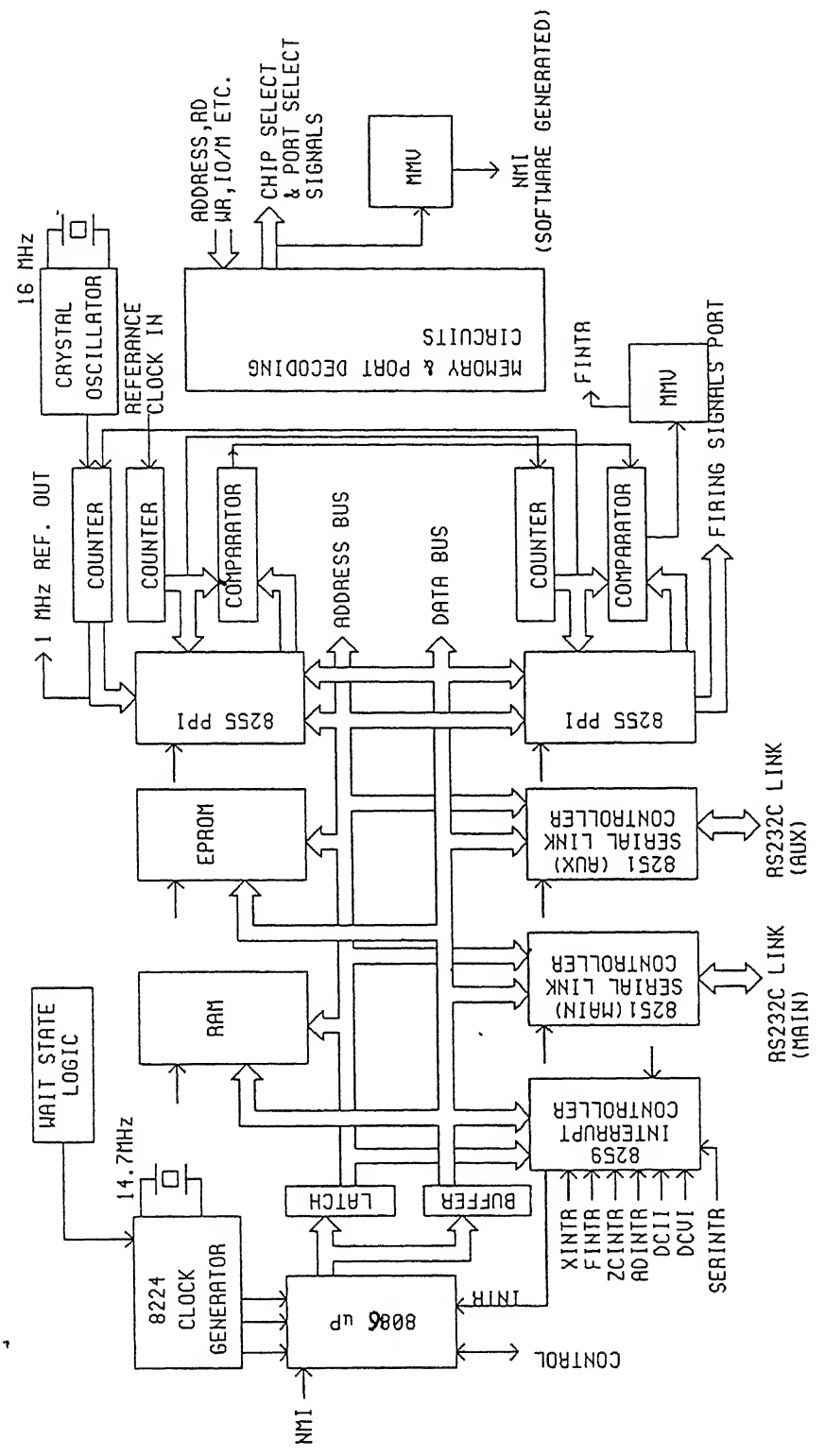

Figure 3.4: Controller card block diagram.

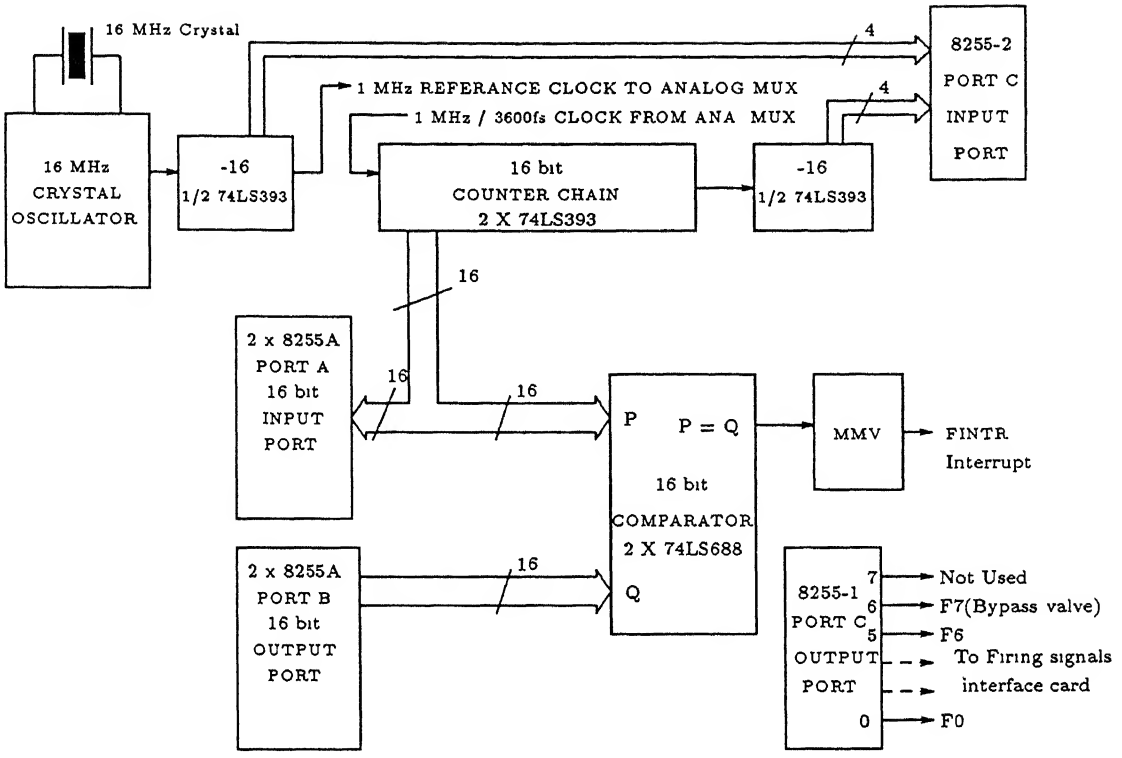

Figure 3.5: Firing signal generation scheme.

suffice for the application. Eight levels of interrupt are provided by 8259A interrupt controller chip. Two 8251A USART chips provide interface for two RS232C links. The hardware is connected for 9600 baud-rate for both the links. Six 8-bit ports are provided through two 8255's. All the six ports are used on-board itself for firing signal generation circuitry.

The firing signal generation scheme is shown in Figure 3.5. It consists of a 16 MHz crystal oscillator, a chain of 24 bit binary divider circuit, a 16 bit comparator circuit and ports provided through 8255's. The 16 MHz signal from crystal oscillator is divided down to 1 MHz by the $\div 16$ counter which is then sent to multiplexer on analog signal processing card-3. Selection between this 1 MHz reference clock and PLL output frequency of nominal value 180 kHz (3600 $\times$ 50 Hz supply frequency) is made by proper control word written on this card. The selected clock signal returns back to divider chain on the controller card where it is fed to clock input of the rest of the 20 bit counter divider chain. The total length of 24 bit counter word is broken into three parts of 8 bits each with most significant and least significant nibbles grouped together to form one byte and

is connected to port C of 8255-2. The middle 16 bits are connected on port A of 8255-1 and 8255-2. As 8255-1 and 8255-2 are connected on lower 8 bit data bus and upper 8 bit data bus respectively, this arrangement allows for reading the 16 bit counter word at one go. Similarly, a 16 bit word can be written to port B of 8255-1 and 8255-2 in one operation. This 16 bit word forms one input to 16 bit comparator whose other input is middle 16 bits of the 24 bit divider chain. On both this words being equal, a firing signal interrupt is generated. This kind of arrangement provides for continuous rolling counter with fast read/write operations. The greatest advantage is that it allows for maximum computation time for inter firing period, the only requirement being that the computation at least be available before the elapse of the time of action it indicates.

Interface to rest of the circuits on the other cards is through I/O ports and 8 bit upper data bus. Upper 8 bit data bus was selected to be able to assign the addresses not used on the peripheral devices connected on the lower data bus.

The serial link interface is provided through two 9-pin D-type connectors at the back edge of the controller card. There are two push buttons on the card, one of which is for system reset and the other is for NMI generation. On system reset and at power on, the system starts executing from FFFF:0000 which is EPROM area. Here, the monitor/debugger program is loaded. The execution of this program activates main RS232C link which is connected to PC serial port. With PC running proper serial link terminal emulation program, the command entry prompt is received from the controller card upon card reset. The user can now issue different commands from the PC. The commands available with present version of debugger are explained in Chapter-4 on the software and is listed with formats in Appendix-C. The user developed programs can be loaded in the controller card RAM using debugger commands and then executed by issuing appropriate commands. Other alternative available is that such a satisfactorily working programs can be burnt into the controller EPROM itself and NMI key can be used to start the application program.

Rest of the circuitry consists of port and memory decoding and addressing circuits. All addresses are assigned in same way as on the 8086 μP kits so that programs developed on it are directly compatible on this card also. All the port addresses can be found in the Appendix-A. Interrupt assignment and memory mapping details can be found in Appendix-B.

3.3 Firing signals interface card circuits

The firing signal interface card takes inputs from port C of 8255-1. The lower six lines are firing signals for valve-1 through valve-6, seventh line is for bypass valve and the most significant 8^{th} line is not used. These are all active low signals with low corresponding to fire signal. These input signals are buffered by 74LS245 at the input. Each signal line is then followed by a couple of NAND gates which mixes hardware inputs for forced ON and OFF signals for each of the seven valves. Thus any valve can be individually kept ON or OFF continuously or for the desired period to simulate a fault. The block diagram of the card is shown in Figure 3.6.

The firing signal path is as shown in Figure 3.7. This sets certain levels of priorities of hardware ON/OFF signals and software generated firing signals. The overall priorities for firing signals are in increasing order from software generated firing signals with lowest priority, followed by hardware forced ON signal and finally hardware forced OFF signal. So signal at the highest level of priority is acted upon. Hardware ON/OFF signals are also active low inputs and can be applied through 8-pole DIP switches placed in the respective sockets or by extending it through DIP header and cable to other hardware circuits which apply the signals for ON or OFF in the manner desired by the user in synchronism with other events as the case may be.

Eighth switch in OFF DIP is for blocking input which, when activated, blocks firing signals to all valves except bypass valve. Both active high and active low blocking inputs are available at the edge connector of the card which can be connected to other circuits like protection circuits. This blocking inputs blocks all gating signals as opposed to individual valve blocking set by the DIP switches.

The eighth switch in ON DIP socket is used to couple internal modulation signal provided by one 555 AMV circuit, which when closed, modulates firing signal by the internal carrier. The same signal is available at $\overline{EXT-MOD}$ pin on the edge connector. When this switch is open, the same pin can be used as input for $\overline{EXT-MOD}$ signal input. With no modulation signal applied, continuous firing signal is available. The other 74LS245 buffer serves to modulate the carrier on all valve firing signal lines by modulating its enable input. The NAND gate which drives enable input of 74LS245 has two inputs. One is for modulating carrier and the other is for blocking signal. This blocking signal line to the gate can be broken and the gate input tied to GND to get simple pulse

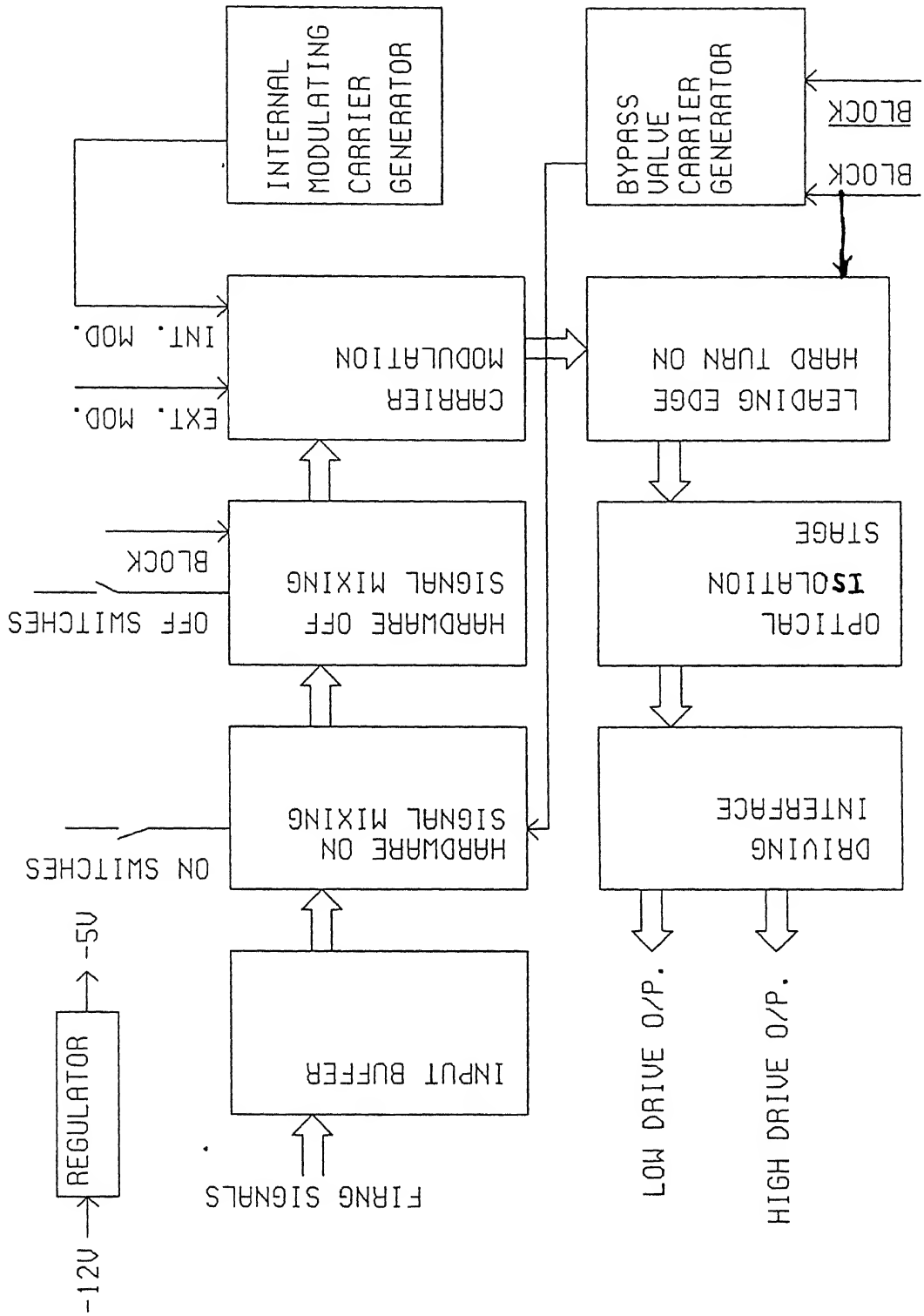

Figure 3.6: Firing signal interface card block diagram.

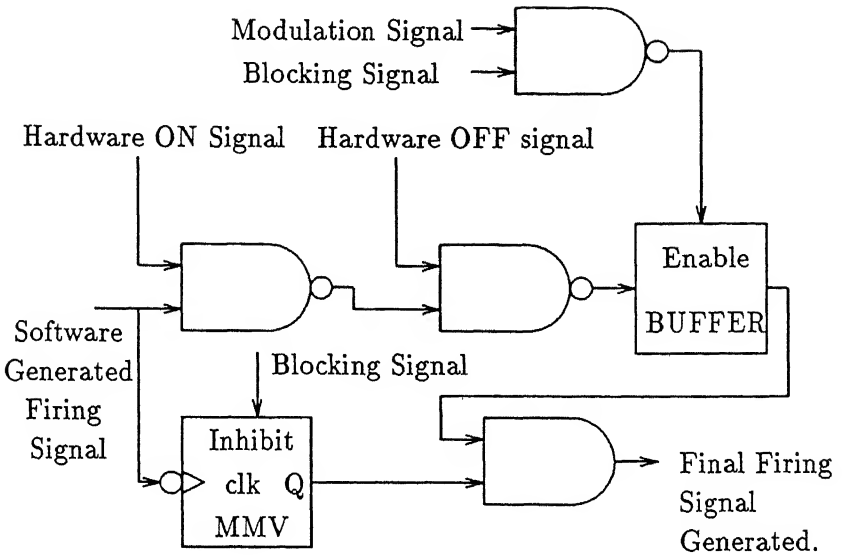

Figure 3.7: Firing signal path.

firing. As HVDC bridges are not used with pulse firing, this mode is not made a regular feature. The firing instant accuracy is maintained even for very low carrier frequency by placing an MMV on each of the firing signal lines. This MMV supplies a pulse at every firing command and irrespective of the status of the modulated output, this pulse reaches final output, as output of MMV is ORed with modulated firing signal. Non modulated continuous signal firing mode should be selected as the pulse transformers used in the given HVDC simulator has large time constant and modulation is redundant.

As bypass valve may be required to operate for large durations and pulse transformers are not capable of sustaining such long pulses, the HVDC simulator uses two pulse transformers each driven by an ac signal with 180° phase difference. This signals are rectified and combined at the output to generate continuous dc signal for bypass valve firing. To make output ripple free, this two 180° phase difference square wave signals are made of duty ratio sightly overlapping in favor of forward direction at firing signal output. Signals of this specifications are generated using 555 astable multivibrator and two op amps from LM324N. Frequency of around 400 Hz is chosen which is not very critical.

The firing signal available at this stage for each of the valves and bypass valves are isolated by eight opto-isolators. This effectively decouples power side transients from entering the control circuitry. The simulator circuits have been built with negative power

supply of –12 V. The logic circuits of the controller designed herewith uses positive supply of +5 V. The opto-isolators interfaces both this logic levels. The supply for the simulator side of the opto-isolators is derived from –12 V available in the firing circuitry of the simulator. One 7805 regulator supplies –5 V as required by the opto-isolators from the same –12 V supply. The driver IC ULN2803A converts switching levels from TTL to 0 and –12 V. The transistors at the output translate firing signal switching levels to that required for pulse transformer driving by inverting this signals. Two sets of drive signals are available, one low drive signal with 100 Ω in series and other direct outputs. In the present application, the low drive is sufficient and hence used.

3.4 Analog signal processing card circuits

This card contains circuits for commutation voltage zero crossing, 12 bit A/D converter with 8 channel analog multiplexer, precision rectifiers for three phase voltages, PLL for generating 3600 times the supply frequency and other interface circuits. The block diagram of the card is given in Figure 3.8.

The commutation voltage signals and interrupt signal at every commutation voltage zero crossings is derived as shown in block diagram in Figure 3.9. Three commutation voltages, corresponding to negative valve group, from the six commutation voltages available from the three center tapped transformers in the HVDC simulator are input to this card. These are then buffered and inverted to generate six commutation voltages by op amp sections A1 and A2 of LM324N's. These six commutation voltages are input to zero crossing detector circuits comprising of six precision comparators LM311N's. The zero crossing threshold for each of the six commutation voltages can be set within small range around GND independently by six trimpots at the edge of the card. A small bias of +25 mV is provided on each input to make it respond only when the actual signal is present. Small hysteresis of 10 mV is provided for noise free crossovers. A small capacitor of 10 nF together with a load resistance of 2.2 kΩ at the output of each of the LM311's also helps in keeping all positive going edges clean. The output of the zero crossing detector circuits goes both to MMV and to voltage status input port provided through 74LS245. Six lines of the port are for voltage status input, seventh line is connected to ADINTR signal which is an interrupt signal generated every 10° of ac cycle. The most significant eighth line is connected to ZCINTR signal which is an interrupt signal generated at every

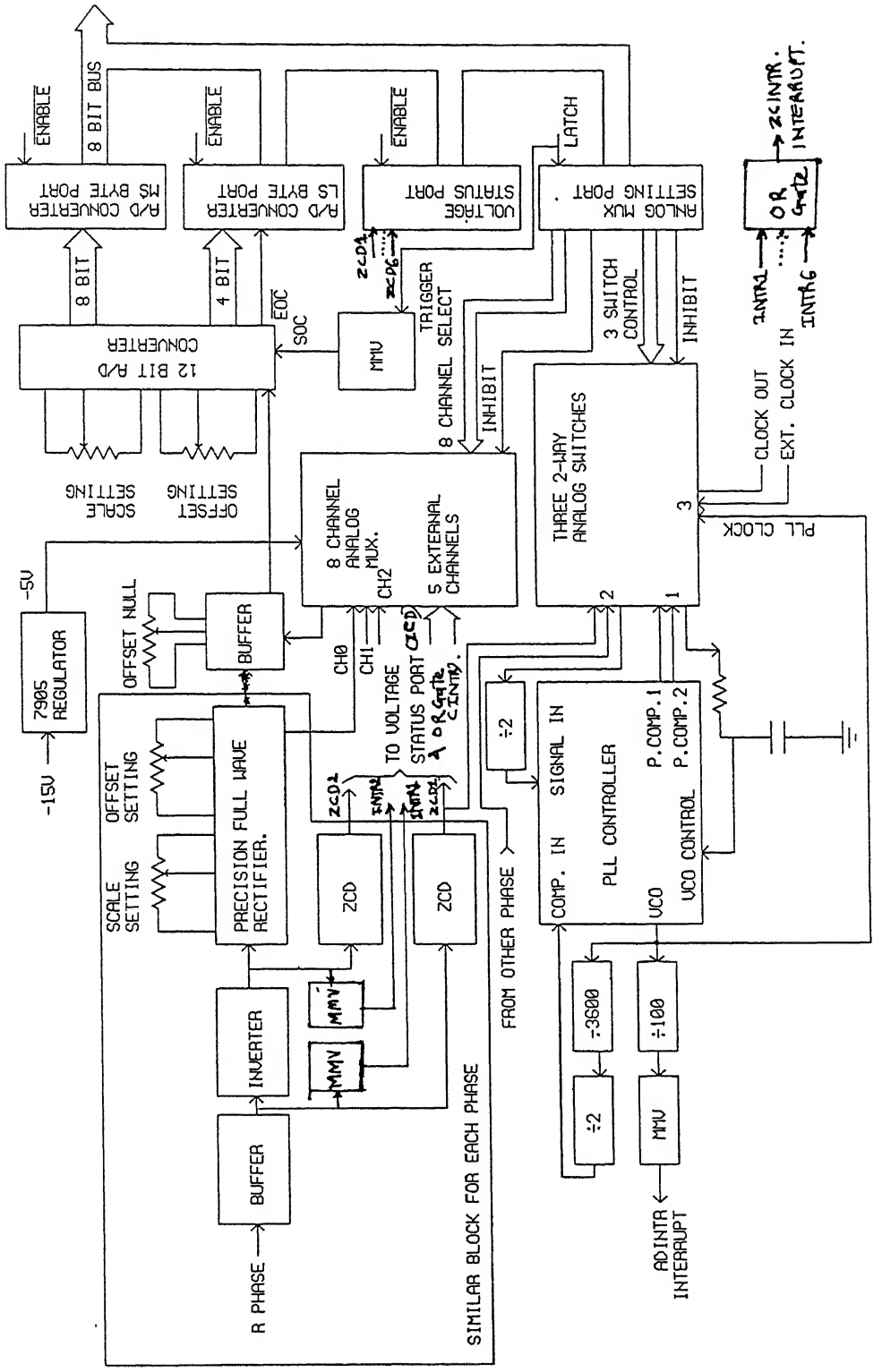

Figure 3.8: Analog signal processing card block diagram.

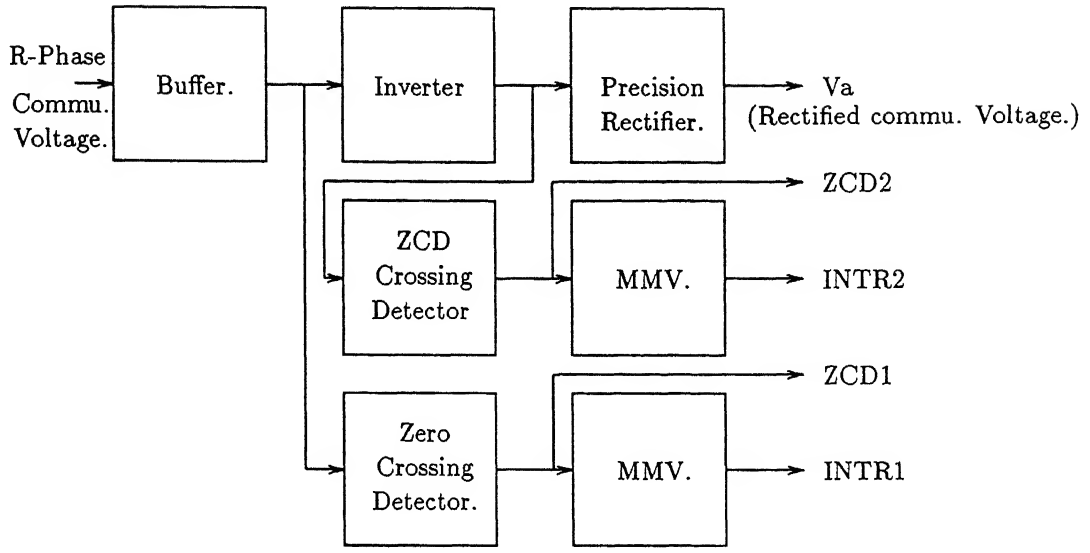

Figure 3.9: Derivation of commutation voltage and its zero crossing interrupts.

positive going zero crossing of any of the commutation voltages. This provides additional flexibility of software polling of the respective interrupt signals if so desired. MMV on each voltage status signal causes pulse at +ve going edge which, for all six voltages, are combined to form a single interrupt ZCINTR through 74LS30 NAND gate.

The block diagram of A/D convertor section and channel multiplexer is shown in Figure 3.10. The three phase voltage signals, after buffering and inversion also goes to precision full wave rectifier formed by two more op amp stages from respective LM324N's. Two trimpots on each of the three rectifiers are used to null offset and for gain calibration. In the present case, the full wave rectified signal is not filtered to dc voltage though the provision has been made for the same. This has been done to keep the high speed sensing of the ac bus voltage possible in case, one wants to incorporate predictive element of correction in CEA control. If this is not required, then signals may be filtered using 25 μF capacitor to get dc voltage proportional to ac voltage for slow response applications. This rectified 3-ϕ ac voltages are applied to ch0–ch2 of analog multiplexer provided by 4051B. The other 5 channels of the 8-channel multiplexer are not used and are available for external use at the edge connector of the card. The edge connectors and other connectors signals are listed in Appendix-D. The supply voltage to the analog mux limits the input signal range between ± 5 V maximum. The analog mux output is applied to fast buffer amplifier AD711 before applying to A/D chip. The 12 bit, 6 μSec A/D converter chip

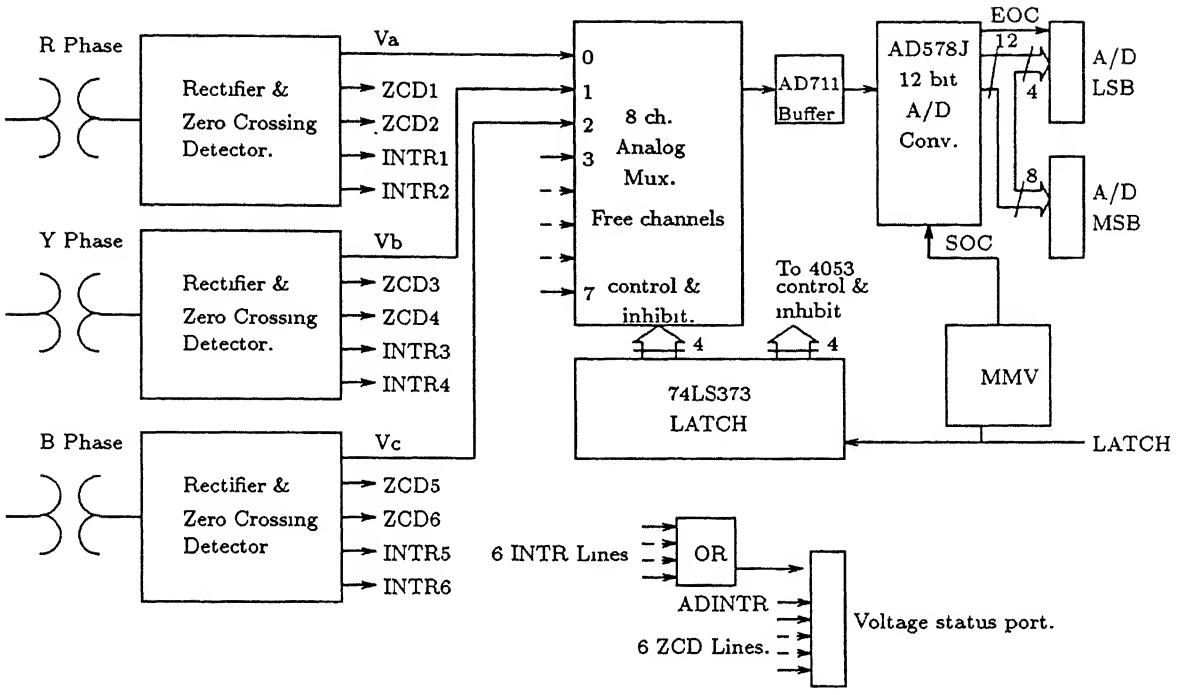

Figure 3.10: Channel multiplexer and A/D converter configuration.

AD578J is configured for bipolar input and has input range of ± 5 V and ± 10 V on two separate pins, both of which are brought at the edge connector. ± 5 V input pin is also connected to output of the fast buffer amplifier AD711. Two trimpots of 100 Ω each are connected to AD578 for offset setting and for scale calibration. The 25 kΩ trimpot connected with AD711 is used for offset nulling. The 12-bit digital output of the A/D converter is not tri-stated and is continuously available. It is connected to the system bus through two input ports provided by two more 74LS245 chips. One is for most significant 8 bits and the other port is for least significant 4 bits on lower nibble of the port along with end of conversion signal-EOC from AD578 at most significant bit position. As the converter chip is very fast with conversion time of the order of 6 μSec, it is not advisable to go in for interrupt approach for EOC.

The other circuit provided on this card is PLL circuit. The configuration for the same is as shown in Figure 3.11. It is designed around PLL controller chip 4046 which is used to generate a reference clock signal which is multiple of supply frequency by a factor of 3600. So the one pulse of PLL output clock corresponds to 0.1° of supply frequency. Thus when this clock is used for driving the counter on the controller card, all angle measurements

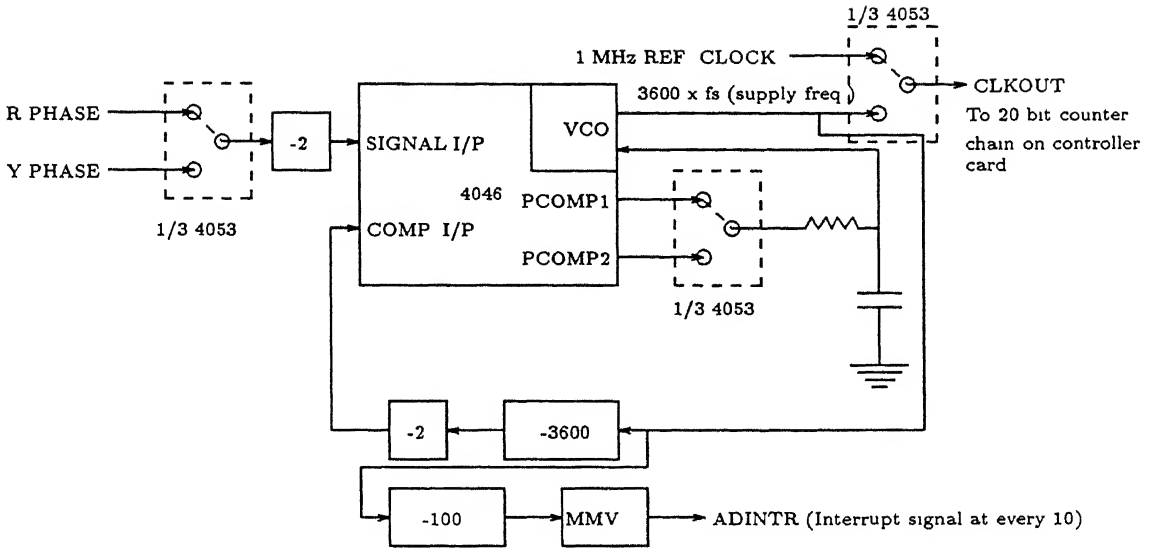

Figure 3.11: PLL configuration.

can be made with a precision of 0.1°. Any frequency variations in the supply are taken care of by PLL and hence calculations needed in the software can be minimized. The PLL has two options for selection of the signal input from either of two phase voltages as a reference. It also has two options for selection of phase error comparators one of which is level sensitive and the other one is edge sensitive. The former is duty cycle sensitive while the later is more stable against locking to harmonics which, anyway is not of much concern as the VCO range has been limited for signals between 40–60 Hz by proper range selection registers. The detailed characteristics analysis of both can be referred through 4046 data sheet. Both of this selections can be made through another mux chip 4053B which provides three, two way analog switches. One of the switch has two inputs coming from output of two zero cross detectors connected on two different commutation voltages in the same group. One of them is selected and is further divided by two by JK flip-flop to make it 50 % duty cycle signal in steady state before applying to signal input pin of comparator in 4046B, which is needed for proper operation of level sensitive comparator. Two phase comparator outputs are available from 4046B, one edge sensitive and other level sensitive. Both of this outputs are applied to another two way switch of 4053B. One of them is selected and is applied to loop filter. This is simple RC filter having time constant of 4.7 msec . So its response would be fast enough for tracking the anticipated

supply frequency variations. The loop filter output goes to the control input of the VCO of 4046B chip. The output of the VCO goes to two divider chains as well as to third switch of analog mux 4053B. The other input to the same switch is 1 MHz crystal based signal coming from controller card. One of the signals is selected and routed back to controller card to be used as a reference clock for 20 bit divider chain that is used for all timing measurements. When the 1 MHz crystal based frequency is used as clock, the resolution obtained is even higher than when PLL based signal is used as a clock but now supply frequency changes has to be compensated in software for angular measurements. Other advantage of the crystal based clock is that as the counter is also used to keep track of other events like for V/F readings. This will not require corrections for supply frequency variations which, in the case of PLL based clock will be needed to preserve the accuracy of the measurements. The two divider chains that are connected to VCO output are for division by 100 and by 3600. The division by 3600 is provided using a 4040B counter chip and few decoding gates for reset control provided by 4073B triple i/p. AND gate. This signal is further divided by two by other JK flip-flop of 4027B to make it 50 % duty cycle signal as in the case of signal input of phase comparator. This signal goes to the other input of the phase comparator in 4046. The other divider chain divides the VCO signal by 100 using 4518B which is then applied to MMV 74LS221N to generate ADINTR signal. This signal is an interrupt signal generated every 10° in the ac cycle and it can be used to sample various voltages through different channels of A/D converter on board. The predictive element of correction in the firing can be easily incorporated by checking ac voltages at every 10° in CEA control.

One more port is available on the card which is an output port provided by one 74LS373. It is to set the two analog mux switch settings. Three channel selection and one inhibit control line of 8 channel analog multiplexer 4051B are controlled through upper nibble. The lower nibble controls switch positions of three, 2 way analog multiplexer 4053B and its inhibit line. One more MMV is also connected to the latch input of this port which gives start of conversion-SOC pulse to A/D converter chip AD578J every time a byte is written to this port. So every new conversion can be initiated by writing appropriate word on this port. This has to be done even when no change in the switch settings is needed. And, as no harm comes of issuing SOC signal even when only switch settings are to be changed, this combining of both functions does not lead to any conflict in the operation.

3.5 Live signals interface card circuits

This card contains circuitry for valve ON-OFF status sensing and for generating valve current extinction interrupt. It also contains two V/F converter circuits for dc voltage and current sensing and an SMPS for generating multiple isolated dc supplies. The block diagram of the card is shown in Figure 3.12.

Valve ON-OFF status is sensed by placing a small 1 Ω resistances in series with each of the valves at the junction point of two valves at ac input terminal or in series with each supply lead to the bridge ac input as shown in Figure 3.13. In the former case, total of six 1 Ω resistances are required and it senses true ON–OFF condition of each valve even when both of them are conducting simultaneously. This connections will require breaking of existing connections of HVDC bridge to insert the current sensing resistances. Instead, here three resisters are used, which are very easy to insert by removing the external links that are used in the HVDC simulator in the supply line of the bridge. The condition of both valves conducting simultaneously can be ascertained by checking the valve ON–OFF status before issuing a firing signal to a particular valve and suitably modifying the logic in such a case. Note that the valve status available on the port exchanges upper valve group with corresponding valve in the lower valve group when connection is changed from three resistor to six resistor sensing and vice versa. For three resistor sensing, both positive and negative valve group inputs for each phase are tied together. The voltage developed across each of the current sensing resistors is given to the zero crossing detector circuits comprising of LM311N's. The LM311N's for the positive inputs gives outputs only for positive input signals and in the same way, negative group gives output for negative input voltage only. The trimpots provided on each ZCD's can be used to set the switching thresholds. The outputs corresponding to both positive and negative groups are applied to two channels of dual opto-isolator HPCL2630's to isolate live circuits from the control circuits. The power source for each ZCD circuits is derived from three isolated ±15 V, 100mA supplies provided by SMPS on board. The output signal from each of the opto-isolators is fed to two MMV's on each signal line. One MMV responds to positive edge and the other responds to the negative edge of the signal. The positive edge triggered MMV output is a pulse of duration of approximately 90° at 50 Hz. This is to block negative triggered MMV output if so selected by discontinuous enable signal which is available at the edge connector of the card. By default, this mode is not selected. This is done to

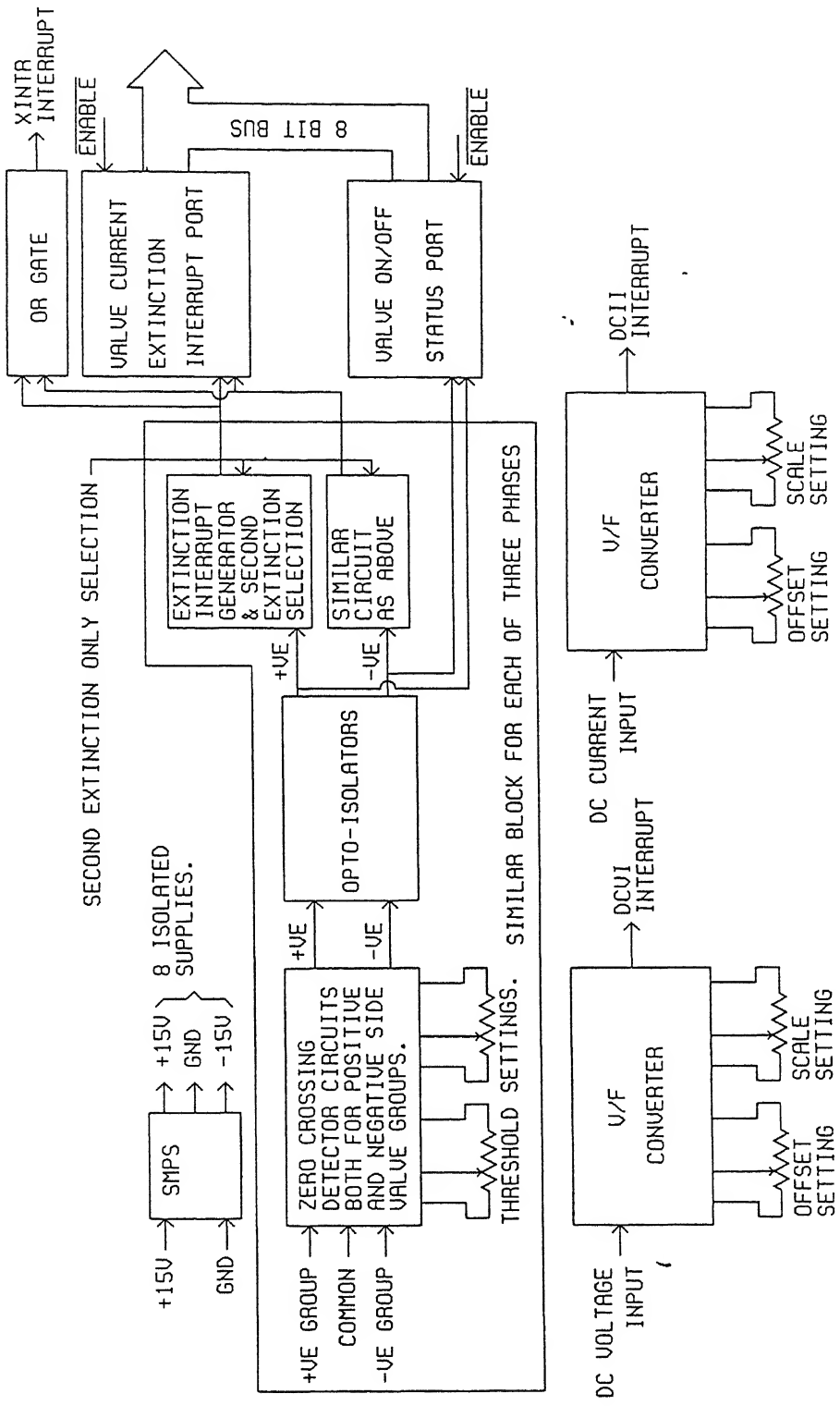

Figure 3.12: Live signals interface card block diagram.

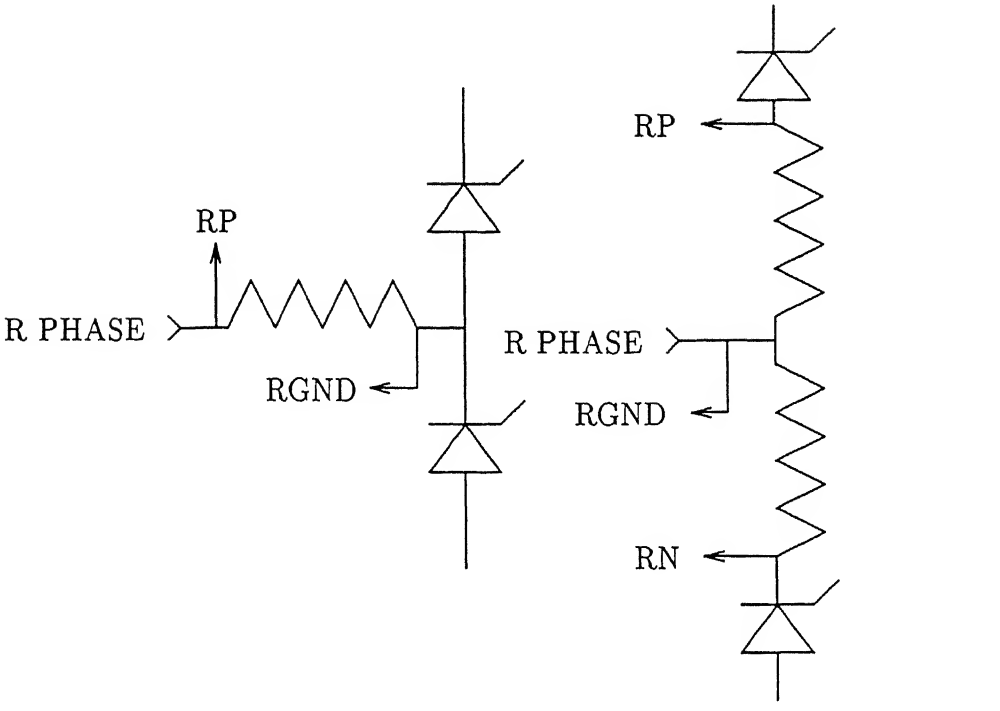

Figure 3.13: Valve ON–OFF status sensing.

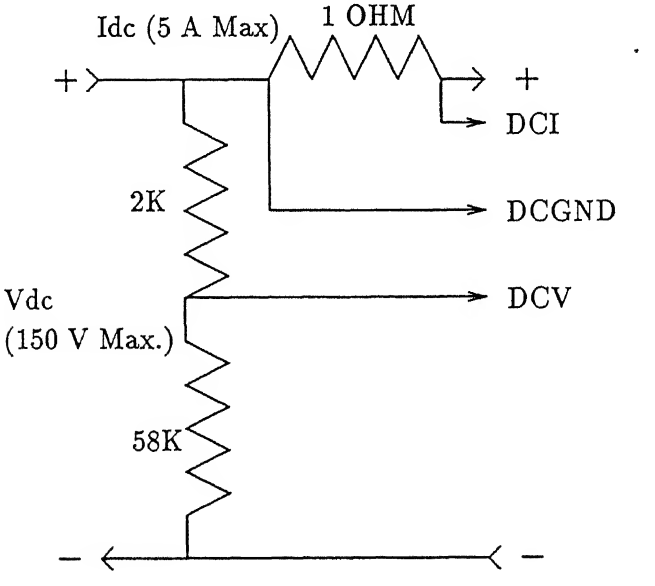

Figure 3.14: DC current and voltage sensing.

ensure that when the bridge operates at very low level of dc current with firing angle more than 60° with discontinuos current then same valve will give two current extinction pulses which is prevented by the other MMV. However if it is desired by the user to have pulse at both current extinctions then that can be selected using active low discontinuos enable signal. The negative edge triggered MMV generates valve current extinction signal. All six such signals are combined using NAND gate 74LS30 to form XINTR signal for valve current extinction interrupt. Two input ports are provided through two 74LS244's, one of which is used to input valve ON–OFF status and the other for reading the interrupt source that caused the interrupt.

Two V/F converters designed around LM331N's are used here to sense the dc voltage and current signals. This was selected in view of ease of isolation that can be provided to frequency signals without the loss of information. The LM331N is extremely fast V/F converter with linearity of the order of 0.03 % of full scale range. The circuit configuration chosen here is standard application of the IC for the purpose with full scale range of 10 HZ to 10 kHZ for a input voltage of 0 to –10 V. This scale factor can be calibrated by 5 kΩ trimpot at the edge of the card. The basic range of 0 to –10 V is shifted to 0 to ±5 V by providing offset of –5 V at the non inverting input of integrator built around op amp section AD712. This –5 V is generated from the reference voltage output of the LM331N which is about 1.9 V, by boosting to desired level and inverting it using another op amp section of AD712. The exact level of offset can be set by 10 kΩ trimpot connected in the feedback loop of this op amp. The frequency output signal from both the LM331N's is given to dual channel opto-isolator HPCL2630. Similar circuitry is used for both voltage and current signal conversion to frequency. The ground of both is made common to reduce the no. of isolated supplies required and hence the current sensing shunt and voltage divider has to be put with common junction as shown in Figure 3.14. Isolated power supply of ±15 V, 100 mA is also derived from the SMPS. The output from the opto-isolators is frequency signal and is used directly to generate dc current signal interrupt DCII and dc voltage signal interrupt DCVI. The DCVI and DCII signals are directly used as interrupt signals. Back conversion to voltage and reading through A/D channels was avoided because of reduction of speed of response due to filtering involved in F/V conversion. And it is very easy to measure the frequency of this signals by taking counter reading at every such interrupt and then voltage or current is calculated by software means.

As has been mentioned, all of the above circuitry required four isolated supplies of ±15 V each capable of supplying 100 mA, an SMPS for the purpose was designed. Providing this voltages through external supplies would have caused wiring clutters and insulation problems. Instead, to keep it clean and self containing on board with few connections, this approach is taken. The SMPS is designed around LM3524 SMPS controller IC and two IRF530 mosfet switches operating from supply of +15V. The configuration used is push-pull, open loop type control. Total eight secondaries are provided which, through use of two half wave rectifiers and filters gives positive and negative dc supplies on each secondary. This are then regulated using 15 V zener diodes on each of the lines. Four ±15 V, 100 mA supplies are not used and are available through four 7-pin connectors and can be used for other purposes whenever requirement for such isolated supply is needed. Extreme caution should be taken while handling this PCB and fifth mother board PCB while the supply is ON as both of them contains live 230 V connections which are taken here for current and voltage sensing. All connectors that connect this PCB with the mother board which are carrying live signals should not be removed or connected with power ON. All trimpot settings on this board should be carried out using properly insulated small screw driver only. While preparing layouts for these PCB's, extreme care has been taken to ensure safe spacings between different phases and DC lines and between other control circuits.

3.6 Mother board circuitry

The only components that go on the mother board are connectors for different purposes, few power supply filter capacitors and one voltage divider for DC voltage, which from the safety considerations was put on the mother board instead of the card that contains V/F converters. This card also contains live wiring and all precautions mentioned for the previous card holds good here too. This card provides all the inter connections between different cards and with the HVDC simulator and with current shunt bank of four shunts. Appendix-D gives the details of the signals that are available on different connectors.

The 44 pin PCB edge connector K10 is meant for plugging controller card. Eight signal lines from controller card marked F1–F8 are valve firing signals that goes to same named signals on the firing signal interface card. The signal lines marked D1–D8 are upper 8 bit data bus of the controller card and it is connected to respective lines with same literals

on analog signal processing card and on live signals interfacing card for different port input and output applications on respective cards. The signals ZCINTR and ADINTR are interrupt inputs on controller card and it comes from analog signal processing card. They are commutation voltage zero crossing interrupt signal and interrupt signal at every 10° for reading A/D channels respectively. The signals XINTR, DCII and DCVI are also interrupt input signals on the controller card and it comes from live signals interfacing card. XINTR is interrupt signal generated at every valve current extinction. DCII and DCVI are interrupts generated by frequency signal output of each V/F converter that is used to sense dc current and dc voltage respectively. The signals LATCH, and active low signals $\overline{E1}$–$\overline{E5}$ generated on the controller card are for port addressing of ports on different cards. LATCH signal is for the only off-card output port which is on analog signal processing card. It is used for analog switch settings. Three other ports on the same card are input ports for commutation voltage zero crossing status input together with ZCINTR and ADINTR signals selected by $\overline{E1}$, upper 8 bits of A/D output selected by $\overline{E2}$ and lower 4 bits with EOC selected by $\overline{E3}$. $\overline{E4}$ and $\overline{E5}$ is for selection of two input ports on live signals interfacing card. $\overline{E4}$ selects port that reads valve ON–OFF status and $\overline{E5}$ selects port that reads valve current extinction interrupt source. CLOCK IN and CLOCK OUT signals on the controller card goes to analog signal processing card with connections to MUXD CLOCK OUT and EXT CLOCK IN respectively. CLOCK OUT signal is 1 MHz crystal clock output and CLOCK IN signal is clock input to run 20 bit counter chain on the controller card. Rest of the three connections on the controller card are power supply connections for GND, +5 V and –15 V.

The 44 pin PCB edge connector K9 is meant for plugging firing signal interface circuit card. O1–O8 and OL1–OL8 signals are output firing signals to drive the pulse transformers. OL-series of signals are low drive signals with 100 Ω resistances in series and they are the one that is used to drive simulator pulse transformers. This set of signal goes to 15-pin terminal strip K1 on the top side of mother board. The other set of output signals O1–O8 are direct drive outputs and they are connected to 34 pin flat cable connector K3 at the bottom side of the mother board which is not used presently. $\overline{EXTMOD}$ signal is modulating carrier input pin when external modulation mode is selected by keeping corresponding switch open. The same signal is output pin to output internal carrier when internal modulation mode is selected. This signal is also made available at 34 pin connector K3 and can be used when required. Two blocking signals are available : one active

high and other active low on firing signal interface card for blocking all the valves of the bridge except bypass valve. It can be used for protection purposes. The active high signal is available at terminal strip K1 where it may be tied with HVDC simulator valve blocking signal which is also active high signal with proper levels and the active low valve blocking signal is available at 34 pin connector K3. GND, +5 V and -12 V signals on firing signal interface card are power supply connections. The -12 V supply comes from HVDC simulator pulse circuit through terminal strip K1. Rest of the lines on connector K9 has already been dealt with.

The 44 pin PCB edge connector K11 is for plugging analog signal processing card. The signals on this connector that are not already explained are three phase commutation voltage inputs Va,Vb and Vc which are input from the simulator through connector K1, CH3–CH7 signals are analog input channels of mux with range ±5 V and are brought on connector K3. Two more signals are ADIP10V and ADIP20V which are 10 V (±5 V) and 20 V (±10 V) unipolar (bipolar) input pins of the AD578. ADIP10V receives signal from buffer amplifier AD711 on that card and is available here also. This two pins can be used as a direct input only when the connection between buffer amplifier and ADIP10V is opened. GND, +5 V, +15V, -15V signals on connector K11 are usual power supply inputs for the card.

The 44 pin PCB edge connector K12 is meant for receiving live signals interface card. All the signals on this connector are covered in the previous sections except $\overline{DISCONT.ENABLE}$ signal which is active low signal for selecting mode in which the discontinuos conduction mode with firing angle more than 60° results in valve current extinction interrupt generated both times valve turns off in usual conduction period of 120°. This signal is made available on the connector K3. By default, in absence of any input on this signal, valve current extinction interrupt is generated only once at the end of usual conduction period of 120° even if the valve had turned OFF two times in the situation explained earlier. GND, +5 V, +15 V and -15 V signals are power connections for the card.

The 44 pin PCB edge connector K8 is free expansion slot where any extension of hardware can be plugged. The only signals that are connected there are GND and +5 V. Rest of the pin has vero board type pattern not connected to anything else.

The 15 pin terminal strip connector K2 which is located on the side of the mother board is used to carry all live signals from the simulator for use in the live signals interface

card. The signal pairs RI-RG, BI-BG and YI-YG are for connection to three, series current sensing 1 Ω resistances in each bridge leads using three resistance connection for valve ON–OFF status sensing. The signals DCI and DCG are for connection across 1 Ω dc current sensing resistance connected in series with dc line. The DCV signal is for connection to a point whose voltage with respect to DCG is to be measured. It is used for DC voltage sensing and has normal range of ±150 V. This voltage is divided down to ±5 volts before applying to live signal interface card by fixed ratio voltage divider that is on the mother board. Other inputs on this connector are GND, +5 V, +15 V and −15 V power supply connections for the operation of the all circuits.

Connectors K4–K6 carry valve current sensing signals to live signals interface card through a piece of a cable and connector at the other end. Similar connection is used to carry dc voltage and dc current sensing signals available at connector K7 to the same card. If one wants to have six resistor sensing for valve ON–OFF signals then all connections are taken from connectors K4–K7 instead of taking it from connector K2, which has provision for two inputs per phase only, whereas three connections are required for each of the phases.

The signals coming on connectors K1 and K3 are already covered in earlier sections. K1 is used to carry signals between HVDC simulator and this controller. K3 has auxiliary signals which are not directly required but may be used as per the needs as it contains many signals that provide additional facilities.

3.7 Interfacing details

Appendix-D gives the details of the signals that are available on different connectors. Five 44 pin edge connectors numbered K8–K12 for card0–card4 on the mother board are for receiving five cards. Four of them as described above and the fifth one on card0 position is for expansion of hardware if required. The four cards are placed in the slots as shown below

- Card1: Firing signals interface card – on connector K9
- Card2: Controller card – on connector K10
- Card3: Analog signals processing card – on connector K11

- Card4: Live signals interface card – on connector K12

The most of the interconnections with the HVDC simulator is provided through connectors K1 and K2, both 15 pin terminal strip connectors. Special kind of connector on fiber board is made for connection at the simulator end which fits into the 4 mm test sockets provided on the simulator. This eliminates need for any wiring changes in the HVDC simulator.

Three multi-core cables carry signals from connector K1 to the simulator. The three groupings are as follows:

Cable1 : V_a,V_b,V_c and –12 V. These are three commutation voltages corresponding to positive valve group and –12 V is pulse circuit power supply. The connector at the end of the cable plugs at the monitoring sockets for commutation voltages and –12 V.

Cable2 : GND, F1–F6. These are common ground connection and six firing signal output to drive the pulse transformers. The links on the simulator that connect the outputs of pulse circuits to pulse transformers are removed and special connector at the end of this cable plugs at pulse transformer inputs.

Cable3 : BLOCK and F7–F8. BLOCK signal is valve blocking signal from simulator and F7–F8 are bypass valve firing signals corresponding to two bypass pulse transformers. The connector at the end of the cable fits into the sockets for bypass pulse transformer inputs which are vacated by removing links that connect internal bypass pulse transformer signal from pulse circuit to pulse transformers. The extra socket below the pulse transformer which is connected to GND may be removed and connected to blocking signal generated in the simulator for connection to BLOCK input to the controller. This takes care of 14 pins, the 15^{th} pin is extra GND which may be left open. Two multi-core cables take signals from controller to simulator and one multi-core cable connects power supply to the controller. The signals in each group are as below. The connections are for 3 resistor valve ON–OFF status sensing.

Cable4 : RI and RG, YI and YG, BI and BG. This are signals across the three current sensing 1 Ω resistances put into 3-ϕ supply inputs to the bridge. The connector at the end of the cable plugs the sockets which are vacated by removing the links that connect the converter transformer secondary to the bridge. The other end of this cable connects to three 1 Ω current sensing resistor bank on the heatsink. A piece of flat cable starts from this resistor terminals and takes signals across this resistors to connector K2. The

resistances are mounted on the heatsink placed on the side of the controller rack in form of bank of four resistances, the fourth one is used for dc current sensing.

A word of caution ! : Make sure that this resistances are properly connected in the circuit before connecting this cable to the simulator else live signals interface card will get damaged due to excessive voltage inputs available on open circuit.

A different arrangement has to be made for six resistor valve current ON–OFF sensing using connectors K4–K6. The simulator circuit will need modifications to insert two 1 Ω current sensing resistors into each bridge arms at valve junction points. Three connections, taken form the junction and two resistor ends are connected to each of the connectors K4–K6.

Cable5 : DCG,DCV and DCI. DCG is DC common point for dc voltage and dc current sensing. DCV and DCI are dc current and dc voltage signals. The links on the simulator that connect bridge output to the transmission line is removed to insert the current sensing resistor and voltage monitor point is tapped using 4 mm plug for dc voltage monitoring. The connections are made such that negative signal is generated for normal current and voltage directions with respect to DCG. A pair of wire is also used to connect to 1 Ω current sensing resistor which is the fourth one on the resistor bank on the heatsink placed on the side of the controller rack. The voltage divider network to drop the dc voltage for V/F input range is on the mother board.

Cable6 : +5 V, GND, +15 V and –15 V. These are power supply connections to the controller. The cable connects proper regulated power supplies to the controller. Capacity of 3 A on +5 V, 2 A on +15 V and 500 mA on –15 V is sufficient for the proper operation of controller.

The 7-pin sockets at the end of the 5 core short cable from each of the connectors K4–K7 carry the live signals from the mother board to the live signals interfacing card in Card4 slot. They plug into the respective 7-pin plugs on that card.

Connector K3 is 34 pin flat cable type plug which carries signals that are listed in Appendix-D is not connected any where as the signals on it are not directly needed for basic implementation of control. They may be connected whenever the need arises for their application.

Connectors K13 and K14 on controller card back edge are 9-pin, D-type plugs used as a main RS232C and aux. RS232C interfaces. They carry T × D, R × D and GND signals on their pins. Two cables connect this to PC and other controller respectively.

Cable7 : GND, main T × D, main R × D. This are main serial link signals that is used to connect to the serial port of the PC. The cable has properly terminated 25 pin D type socket at other end to connect it with PC COM port and 9 pin D type socket at controller end to fit the plug. The T × D and R × D lines is to be cross connected between the two units.

Cable8 : GND, aux T × D, aux R × D. This is common cable between the two controllers and hence only one unit is needed. It has 9 pin D type sockets at each end with T × D and R × D lines cross connected.

This finishes the hardware circuitry and inter connection description. The Appendix-A to F may be consulted for any specific details regarding this.

Chapter 4

Software description

4.1 Software organization

The software for the HVDC simulator controller can be divided into two parts, one EPROM resident monitor/debugger program and other RAM or EPROM resident user application program. The monitor program is essential to run the services of the controller card and it facilitates the user program developmental work by allowing loading, checking register/memory contents, execution with single stepping or break point facilities and other such utilities. The user program is application program developed for the operation of HVDC simulator controller. It deals with the control and simulation requirements of the simulator.

4.2 Monitor/Debugger program

4.2.1 General

This program starts execution with system reset and it takes commands from main RS232C link which is connected to the PC serial port. This program helps the user in application program development. It has facilities for dumping register or memory contents, memory block moves, memory/register content modifications, port input and outputs, execution with or without break points or single stepping etc. The program is organized as main line program and routines for different services, some of which are directly accessible by the user and others are for access by other routines.

4.2.2 Main line program

The program starts by clearing the interrupt flag and then initializes the stack to 0100:1000 and data seg at 0100:0000. Then main and auxiliary RS232C serial link controllers are initialized for 2 stop bits, parity disabled, 16 baud rate factor and auto reset. This baud rate factor along with hardware connections results in baud rate of 9600. The interrupt vectors for single stepping interrupt INT1 and break point interrupt INT3 are set to proper values. NMI vector is set to F000:0000 which is the start address of the EPROM on board. NMI can be generated both by hardware means using push button provided for the purpose and also by software means by reading from port FFF7. Then vectors for various user services are loaded into routine address table which, by default contains address for the do_nothing routine which does nothing except generating appropriate message and simply returns back to main line program. As each command for the debugger starts with a capital letter from alphabet, total 26 of them are there, only few of which are actually used. Rest may be used as the need arises by loading proper address vector in the routine table. The program then sends initialing messages concerning the usage of the debugger. This ends the non repetitive portion of the program. Now the program sends the command prompt and waits for the user response. The user command entry is terminated by CR in all cases except memory substitution command in which case, comma terminates the command to keep compatibility with μP kit substitution command. This ensures that same loading program can be used here also. After the complete command entry, appropriate service routine is selected and executed. After the execution of the routine, the control returns back to the command prompt sending. All the commands to the monitor program starts with letter in the range A-Z with one letter immediately following it in few cases as a modifier . One or more optional arguments may follow the command as the case may be. Items shown in the square brackets are optional inputs and asterix postfix is used to show repeated usage.

4.2.3 Register display/modify service routine

The command syntax for this command is :

R[N][,]*

N is an optional hex number between 0-D. When no number is specified, all register contents are displayed and control returns back to main line. When number specifier

follows, then that numbered register is displayed and then user response is awaited. The registers are numbered in the sequence AX,BX,CX,DX,SP,BP,SI,DI,CS,DS,SS,ES,IP and Flag register from 0-D hex numbers. If user responds by comma entry, then next register is displayed and like wise, till flag register is displayed. Any valid alpha-numeric number entered will replace the existing value of register and next register will be displayed. This can be continued till flag register is displayed. Any response other than this two, will act as a routine terminator and control will return back to main line.

4.2.4 Dump memory service routine

This routine displays memory contents byte wise, with at most 16 bytes on a line. Each line starts with segment and offset value. The command syntax is as shown below :

Command line	Memory addressed	
	From	To
D [Seg][:][Offset1][,][Offset2]	Seg:Offset1	Offset2

4.2.5 Substitute memory service routine

The command syntax is as follows :

Command line	Memory addressed
S [Seg][:][Offset][,]*[byte,]*	Seg:Offset

Note that the comma is used as a command terminator. The existing byte is displayed along with it's offset and user response is awaited. If user responds by comma entry then next location is displayed without any changes to the previous one and again waits for user response in the same loop. If user supplies a valid number then that value is used to substitute the original value. If comma was entered as number string terminator then next value is displayed in the same way else the routine is terminated. Any entry other than the above two will also terminate the routine and the control will return back to the main line program. This command provides the service which is used by the down loading program to load user program into the controller card RAM.

4.2.6 Move memory block service routine

The command syntax is as follows :

M [Seg1][:][Value1][,][Value2][,][Seg2][:][Value3]

Source		Destination
From	To	At
Seg1:Offset1	Offset2	Seg2:Offset3

4.2.7 Do_nothing routine

This is the default service routine for commands that are not defined. It only displays the error message and returns to main line program.

4.2.8 Input service routine

The command syntax is :

I[W] [port][,]*

The default port used is DX and default size of the port is byte. If W immediately follows, then word size input is taken. Input is taken from the port if any specified on the command line else default port is used. The value input is displayed and user response is awaited. Comma entry is for next input to be taken and displayed in the same loop. Any other response terminates the routine and returns to the main program.

4.2.9 Output service routine

The command syntax is as follows :

O[W] [DX] [,data]*

Here too, default port used is DX and port size is byte size. If W specifier follows, then the word is output. It waits for the data input if not specified on the command line. Any other response than the comma input, will terminate the routine. Comma will start data string which ends on first non alpha-numeric character. This data is output on the port and again the user response is awaited in the same loop.

4.2.10 Execute service routine

The command line syntax is :

Command	Effect → Jump To
G [Seg][:][Offset1][,][,Offset2]	Seg:Offset1 (with break point at Offset2)

This routine saves the monitor program register and stack values in the data segment for resumption of register values after return from user program execution. It then gets the address where to jump for user program execution by values specified on the command line or by using default values. A comma following the jump address followed by an address offset on the command line sets the break point at that address by replacing that instruction with INT3 - CCh instruction. A break point set indicator flag is set to be used after return to restore the original instruction. If no address follows the comma, then single step execution is set by setting trap flag before jumping to the user program. Before actually jumping to the user program, the stack is set to the required values and whole environment of register values with which the program execution is desired is pushed on the stack starting with the jump address and flags followed by all register values. Then all register values are set to that values by popping from the stack with IRET instruction at the end which will restore flag register and jump to desired program.

Now if either single stepping or break point is selected, then the program execution will return back to monitor program after appropriate software interrupt. The vector for both single stepping interrupt and break point interrupts is set to same address. When control returns to this address, data segment is restored to it's monitor program value and all register contents returned from the user program execution are saved. It then restores the stack to it's original last used values in the monitor program. Then if return was from break point, the original instruction at the break point address is restored. Then indicator for break point execution is reset and trap flag is also reset. The register values returned from the user program are then displayed and response from the user is awaited after sending second command prompt. This particular complicated sequence is followed to decouple the influence of the user program from the monitor program and vice versa. It ensures clean interaction between the two programs. The only restriction that is imposed is that the user program specified stack values should be valid to be used and the user program should make balanced use of the stack. At second command prompt, the user may continue single step execution by comma entry or execution with break point by

comma entry followed by next break point and like wise in the same repetitive fashion. Any user response other than comma, after the prompt will terminate the routine and control will return back to the main line program.

4.2.11 Help service routine

This routine displays a short commands usage message and then returns back to main line program.

4.2.12 Other routines

Other routines that are not directly accessed by the user but are used by the other program routines are as follows.

Addr_ascii routine is for conversion from word to ascii string. The address (word) is in AX and the string is returned in addr_out.

Byte_ascii routine is for conversion from byte to ascii string. The byte is in AL and the string is returned in byte_out.

Strout routine outputs ascii string on main RS232C port. The string is terminated by $. Input string is pointed by [BX]. For any carriage return character 0DH in the input string, line feed 0AH is automatically inserted.

This finishes the description of the monitor/debugger program having discussed all major portions of the program individually. The program is actually loaded in EPROM1 and EPROM2 with starting address FD00:0000 to FF00:0FFF. Upon system reset, the instruction at FFFF:0000 is executed which is a jump instruction to the start of monitor program loaded at FD00:0000. Upon execution of this program, data segment is initialized at 0100:0000 and stack is initialized at 0100:1000. Thus whole area upwards to 0200:0000 is available for the user programs. Also, by default, the NMI vector is set to F000:0000 and hence, application program may also be made EPROM resident at this address for execution after hardware or software generated NMI interrupt.

4.3 Converter control program (CFA type)

The algorithm is based on equidistant firing control. Firing pulses are generated at every 60° in steady state. Firing angle is measured every cycle and compared with set value .The

difference is used to correct the next firing. Thus it implements feedback type constant firing angle control. As the error term is used to correct one particular valve firing only, with all other valves fired at 60° interval, it is basically EPC type of firing control. Whenever control action demands change in the firing angle, a signed correction is added to 60°.to get new inter firing period. The basic signals needed for the implementation of the scheme are commutation voltage zero crossing interrupts and firing interrupt generated by counter after set delay. All of these are provided by the circuits designed. The interrupt assignments and memory address details are as shown in the appendix B. The port address details can be found in the appendix A.

4.3.1 Program organization

The whole program is broken down into modules, each one dealing with different interrupt service for ease of program understanding and testing. The program module f0.asm contains main line program and modules f1.asm and f2.asm for commutation voltage zero crossing interrupt servicing and for servicing firing interrupt generated by counter at set value. The file pr.h is a header file containing all definitions used throughout the program. We will describe the functions of each modules one by one in the following sections.

4.3.2 Main line program

The program structure is built on the lines of the main line program of the monitor/debbuger program. Some of the routines used there are used here also. Few routines are added for providing some new servies as demanded by the control program. Complete data structure and stack are defined in this module. The main line code contains instructions for segment, interrupt vector and various peripheral chips initialization. After initializing the chips, the analog mux on analog signal processing card is set for crystal clock, Vca as a reference.

Then some initialising message and command prompt is sent on the main serial link. Now the main line program enters infinite loop which continuously checks availability of characters on the main serial port and for any error messages returned from any interrupt service routines. If any message is returned from interrupt service routine, then it is sent on the main serial link. Any command string issued by user is interpreted at carraige return just like main line program of monitor/debugger program. Valid command is

executed by jumping to appropriate service routine and return value from the routine is displayed or appropriate error message is generated.

H : Help is available by this command.
The program variables can be viewed by display command which has a syntax as follows :

D[V][offset]
Where V is any variable from F-for firing angle setting, M for ON/OFF mask or I for interfiring period. Alternatively, an offset may follow D to view any variable in the data segment with given offset. The offset value can be had from the listing of the data segment.
The program variables can be set by command S which has a syntax as follows :

S[V][value][U]*[D]*
Where V is the name of the variable that is to be set. It can be F for firing angle referance, M for ON/OFF mask setting. The variable to be set is replaced by the value that follows. If the no value follows, no change is made. In case of firing angle setting, if no value is specified, the program waits for some time to check for pressing of U or D keys which can can be pressed continuously for continuous up/down of the firing angle. At every press of the key, 1° change is made in the firing angle.

G : To start the bridge operation.
At this command, some initialising checks are made on the system and if every thing is all right, then the bridge operation is started. The checks include availability of ac commutaion voltage at voltage status port and its phase sequence. Execution starts only with correct phase sequence A-B-C. It then waits for Vac zero crossing. On Vac zero crossing, a delay corresponding to set value of firing angle (the default being 30°) is set on the timer, sets interrupt flag and then returns back to main line program.

Few routines like hex2dec and dec2hex are added for hex to decimal and back conversion to provide better user interface. This finishes main line code.

4.3.3 Firing interrupt FINTR handling routine

Upon elapse of set time on the timer, this interrupt is generated and this routine starts execution. Records are made for the count at firing, last valve fired etc. Now if the last fired valve was valve no.6, then actual alpha is calculated and compared with referance alpha. The difference term is used as a correction in the next valve firing. If the last fired

valve was any other valve than valve no.6, then correction term is set to zero. Then set_counter routine is called to set next firing instant.

The set_counter routine in this module sets next firing instant. It takes signed word in register AX as a correction in the interfiring period to be added with count corresponding to 60° and adds this value to count at last firing. This value is used to set the timer which will give FINTR interrupt at that instant.

4.3.4 Zero crossing interrupt ZCINTR handling routine

Upon execution of this routine, counter reading is taken and stored with appropriate commutation voltage. If the last valve zero crossing was that corresponding to valve no.6, then cycle period is counted by taking the difference with count at same zero crossing. This is divided by 6 and is used to set count_60d value which is interfiring period for next cycle. Also set are half cycle count value count_180d and count corresponding to 1° in count_ 1d by taking appropriate divisions.

This finishes the description of converter control program. This serves only as a structure on which the program may be built/enhanced rather than the fully fledged software on its own.

Chapter 5

Concluding remarks

5.1 Test results and conclusions

The feedback type constant firing angle-CFA control program, as described in the previous chapter, was compiled and loaded in the controller card RAM, using a downloader program through main RS232C link. This downloaded program was then executed by issuing proper commands. With correct phase sequence of the 3-ϕ supply, the bridge starts operation with default firing angle of 30^0. The waveforms obtained for the same is shown in Figure 5.1. Now different firing angles were set using set firing command-SF. Firing angle was also varied continuously by U/D keys. With set mask command-SM, a mask was set for blocking the firing pulses of one valve continuously. The waveforms obtained are shown in Figure 5.2. Next, the original program was modified so that the interfiring period is not exactly 60^0. So the firing angle will continuously sweep over the whole range. This effectively demonstrates a crude form of power modulation.

[illegible] Figure 5.3

So as can be seen, the system is quite flexible and fully programmable. As the compiled programs can be directly loaded into the controller card RAM for the execution, the program developmental time is reduced. Thus, it indeed provides a hardware platform on which HVDC system control and simulations can be carried out. The whole system acts as a link between software simulations and actual HVDC systems. The real time run of the actual scheme can throw more light on the feasibility of the scheme. As the things happening can be actually viewed on this scaled down system, the physical feel of the HVDC systems is maintained.

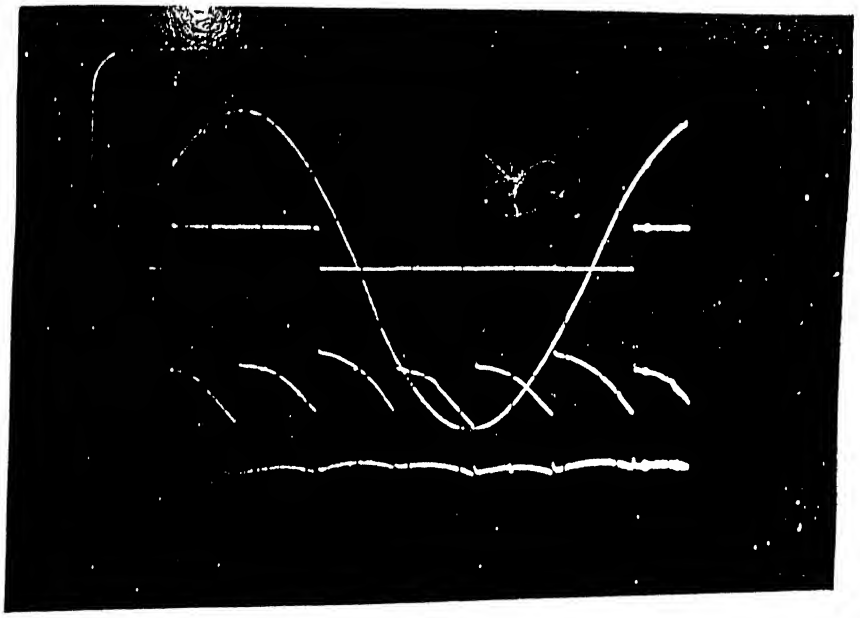

Figure 5.1: Waveforms obtained at α=30^0.

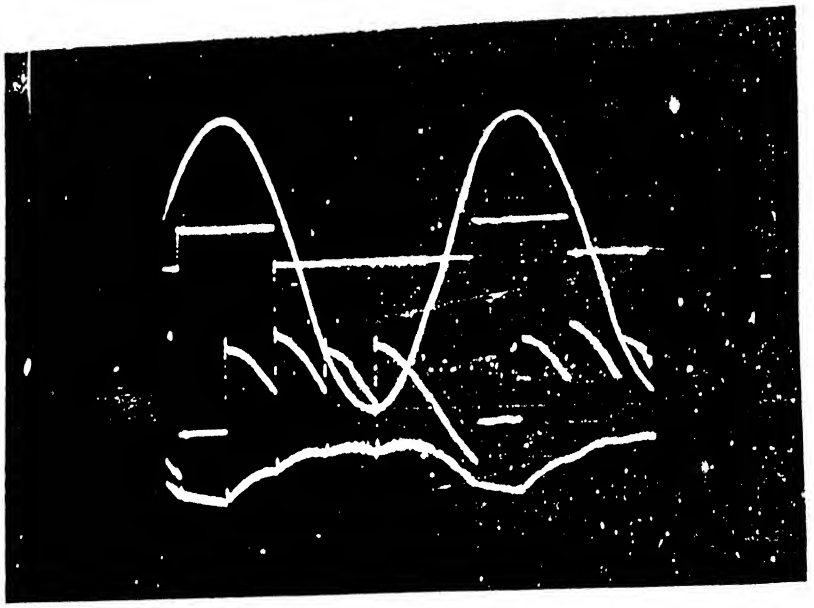

Figure 5.2: Waveforms obtained at α=30^0, with one valve pulses blocked.

5.2 Recommendations for further work

The hardware has provision for adding one more expansion card in the slot card0. This may be used to add protective circuits which, present design depends upon signals from the simulator. It may contain the hardware fault synchronizing circuits to apply faults at particular external event. The external event may be input from two bits free on ports on live signals interfacing card. Also two more port decoding lines are not used on the controller card which may be brought out and two 8-bit input ports may be added if needed. The existing manual on-load tap changing control may be replaced by automatic tap changer control which can be controlled by program in coordination with firing angle control for optimization of reactive power demand. On the software side, there is a scope for lot of work as was mentioned in the last section of chapter 4. The existing constant firing angle control, written to demonstrate the project work, can be enhanced by replacing the feedback type CFA control with HVDC bridge control software. The paper dealing with this by N.L.Shore and L.L.Freris [2] can be an excellent starting point. In fact, a program implementing that algorithm was written and is available in files m0.asm through m7.asm. Due to lack of time available, that could not be debugged and installed. It will need a bit of debugging and writing code for linearizing CC control to put it working. The user interface is to be designed for providing the control and simulation commands. Digital storage scope function with fault preview facilities can be incorporated. Different converter control strategies can be designed and tested. Voltage control of the converter terminal can be implemented by control on reactive power drawn by the converter. Use can be made of the spare channels available on the A/D converter.

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[2] N.L Shore and L.L. Freris.'Minicomputer online control of link convertors', IEE Proc. Vol.125,No.3, March 1978.

[3] J. Arrillaga and G. Galanos. 'Theoritical basis of a digital method of grid control for HVDC convertors '.IEEE Trans.,Vol.PAS-89,No.8,Nov.-Dec.1970.

[4] J.Arrillaga, G. Galanos and E.T. Powner. 'Direct digital control of HVDC convertors'. IEEE Trans.Vol.PAS-89, No.-8, Nov.-Dec.1970.

[5] K.R. Padiyar. ' HVDC power transmission systems-Technology and system interactions'. Reference Text published by Willy Eastern Ltd.New Delhi.

[6] A. Hammad, K. Sadek, H.Koelsch and G. Gueth. 'Advanced scheme for voltage control at HVDC converter terminals'.IEEE Vol. No.PAS-104,No.3, March 1985.

Appendix A

Port addresses and their functions

Chip No.	Port	Address	Function
8255-1	Port A	FFF8	Least significant byte of counter–Input
	Port B	FFFA	Least significant byte of timer setting–Output
	Port C	FFFC	Firing signal outputs–Output
	Control	FFFE	Control/status register–I/O
8255-2	Port A	FFF9	Most significant byte of counter–Input
	Port B	FFFB	Most significant byte of timer setting–Output
	Port C	FFFD	Least significant and most significant nibbles of counter–Inp
	Control	FFFF	Control/status register–I/O
8259	CW1	FFC8	Control/status register1–I/O
	CW2	FFCA	Control/status register2–I/O
8251-1	Control	FFD0	Control/status register of aux. serial link–I/O
	Data	FFD2	Data register of aux. serial link–I/O
8251-2	Control	FFF0	Control/status register of main serial link–I/O
	Data	FFF2	Data register of main serial link–I/O

Chip No.	Port	Address	Function
74LS245	ZCSTATUS	FFD1	Commutation voltage zero crossing status–Input
74LS245	ADMSB	FFD3	A/D converter most significant 8 bits–Input
74LS245	ADLSB	FFD5	A/D converter least significant nibble and EOC–Input
74LS244	VSTATUS	FFD7	Valve ON-OFF status reading–Input
74LS244	XISRC	FFF1	Valve current extinction interrupt source–Input
	NU-1	FFF3	Not used–Input
	NU-2	FFF5	Not used–Input
	NMI	FFF7	Any read from this port generates NMI–Input
74LS373	LATCH	FFD1	Analog mux. switch settings–Output

Appendix B

Interrupt assignments and memory map

Interrupt No.	Signal Name	Usage
IR0	NU	Not used.
IR1	FINTR	Counter interrupt generated at end of set time.
IR2	XINTR	Interrupt generated at every valve current extinction.
IR3	ZCINTR	Interrupt generated at every voltage zero crossing
IR4	DCII	Interrupt generated by frequency signal of V/F converter used for dc current sensing.
IR5	DCVI	Interrupt generated by frequency signal of V/F converter used for dc voltage sensing.
IR6	ADINTR	Interrupt signal generated every 10° of input ac cycle to take voltage samples.
IR7	SERINTR	Interrupt generated by either of the serial links when any character is available for reading

MEMORY AVAILABLE :

00000H – 0FFFFH : On-board RAM provided by 62256-1 and 62256-2

F0000H – FFFFFH : On-board EPROM provided by 27C256-1 and 27C256-2

MEMORY USAGE :

00000H – 00FFFH : Reserved for interrupt vectors and other details.

01000H – 01FFFH : Used for data and stack segments of monitor/debugger program.

02000H – 0FFFFH : Available for user programs.

F0000H – FEFFFH : Available for storing permanent user programs.

FF000H – FFFFFH : Monitor/debugger program stored.

Appendix C

Monitor/debugger commands syntax and usage

Optional values are shown in [] and * postfix is used to indicate that repeated entries of the previous argument is possible.

R[N]
To dump register contents if no N is specified. N is hex number in the range 0–D to display N^{th} register value and modify it if new value is entered. Numbering is in sequence AX,BX,CX,DX,SP,BP,SI,DI CS,DS,SS,ES,IP and Flags. Works in loop with comma entry for next register display/modification.

D seg:offset1,offset2
To dump memory contents from seg:offset1 to seg:offset2.

S seg:offset[,]*[data1,]*
To substitute memory contents at seg:offset by data1. Subsequent locations can also be replaced by entering successive data after comma.

M [seg1][:][offset1][,][offset2][,][seg2][:][offset3]
To move a block of memory between seg1:offset1–seg1:offset2 to seg2:offset3.

I[W] [DX][,]*

Takes input from port DX. DX is default port when no port is specified and W specifier is for word input. Runs in loop taking new input with every comma input.

O[W] [DX] [,data1]*

To output on port DX. Works in the same way as input command except for the extra data field provided.

G [seg][:][offset1] [,]*[offset2]*

To execute program at seg:offset1. Comma terminator with offset2 for break point at offset2 and no address after comma for single step execution.

H : To display short help message showing commands syntax.

Appendix D

Signals on different connectors

Table D.1: Signals on diffent connector pins

Pin No.	Connector No.				
	K1	K2	K4	K7	K13
1	Block	RG	RP	DCI	NC
2	F8	RI	RN	DCV	RXD
3	F7	YG	RGND	DCGND	TXD
4	GND	YI	RVS+	DCVS+	nc
5	F6	NC	RVS–	DCVS–	GND
6	F5	–15V	NC	-	-
7	F4	+15V	NC	-	-
8	F3	GND	-	-	-
9	F2	+5V	-	-	-
10	F1	NC	-	-	-
11	GND	BG	-	-	-
12	Va	BI	-	-	-
13	Vb	DCG	-	-	-
14	Vc	DCI	-	-	-
15	–12V	DCV	-	-	-

Table D.2: Signals on PCB edge connectors (A-solder side, B-component side)

Pin	Card1		Card2		Card3		Card4	
No.	A	B	A	B	A	B	A	B
1.	BLOCK	F8	NC	-15V	CH3	LATCH	+5V	DCVI
2.	$\overline{BLOCK}$	F7	NC	NC	CH4	+5V	+5V	DCII
3.	$\overline{EXTMOD}$	F6	NC	NC	CH5	+5V	+5V	D6
4.	GND	F5	+5V	GND	CH6	+5V	$\overline{E5}$	D5
5.	GND	F4	+5V	GND	CH7	+5V	$\overline{E4}$	D4
6.	GND	F3	+5V	GND	Va	GND	XINTR	D3
7.	GND	F2	D1	CLKIN	Vb	GND	GND	D2
8.	-12V	F1	D2	CLKOUT	Vc	GND	GND	D1
9.	-12V	+5V	D3	$\overline{E5}$	EXTCLK	GND	GND	$\overline{DIC.EN}$
10.	NC	+5V	D4	$\overline{E4}$	CLKOUT	$\overline{E3}$	+15V	+15V
11.	NC	+5V	D5	$\overline{E3}$	D8	AD10V	+15V	+15V
12.	NC	NC	D6	$\overline{E2}$	D7	AD20V	NC	NC
13.	NC	NC	D7	$\overline{E1}$	D6	NC	NC	NC
14.	NC	NC	D8	LATCH	D5	NC	NC	NC
15.	OL1	O1	NC	NC	D4	NC	NC	NC
16.	OL2	O2	F7	F8	D3	NC	NC	NC
17.	OL4	O3	F5	F6	D2	ZCINTR	NC	NC
18.	OL3	O4	F3	F4	D1	ADINTR	NC	NC
19.	OL5	O5	F1	F2	$\overline{E2}$	$\overline{E1}$	NC	NC
20.	OL6	O6	XINTR	NC	+15V	-15V	NC	NC
21.	OL7	O7	DCII	ZCINTR	+15V	-15V	NC	NC
22.	OL8	O8	ADINTR	DCVI	+15V	-15V	NC	NC

Appendix E

Detailed circuit diagrams

The detailed circuit diagrams of all the four major cards excluding the motherboard are attached in the form of schematic sheets totalling four in numbers. They follow in the following sequence :

1.Firing signals interface card circuit schematic.

2.Controller card circuit schematic.

3.Analog signals processing card circuit schematic.

4.Live signals interface card schematic.

Figure E.1: Firing signals interface card schematic.

Figure E.2: Controller card schematic.

Figure E.3: Analog signal processing card schematic.

Figure E.4: Live signals interface card schematic.

Appendix F

Component and connector locations on the cards

The components, trimming pots and connectors can be located from the card layouts attached herewith in the following sequence :

1.Firing signals interface card layout.

2.Controller card layout.

3.Analog signals processing card layout.

4.Live signals interfacing card layout.

5.Mother board layout.

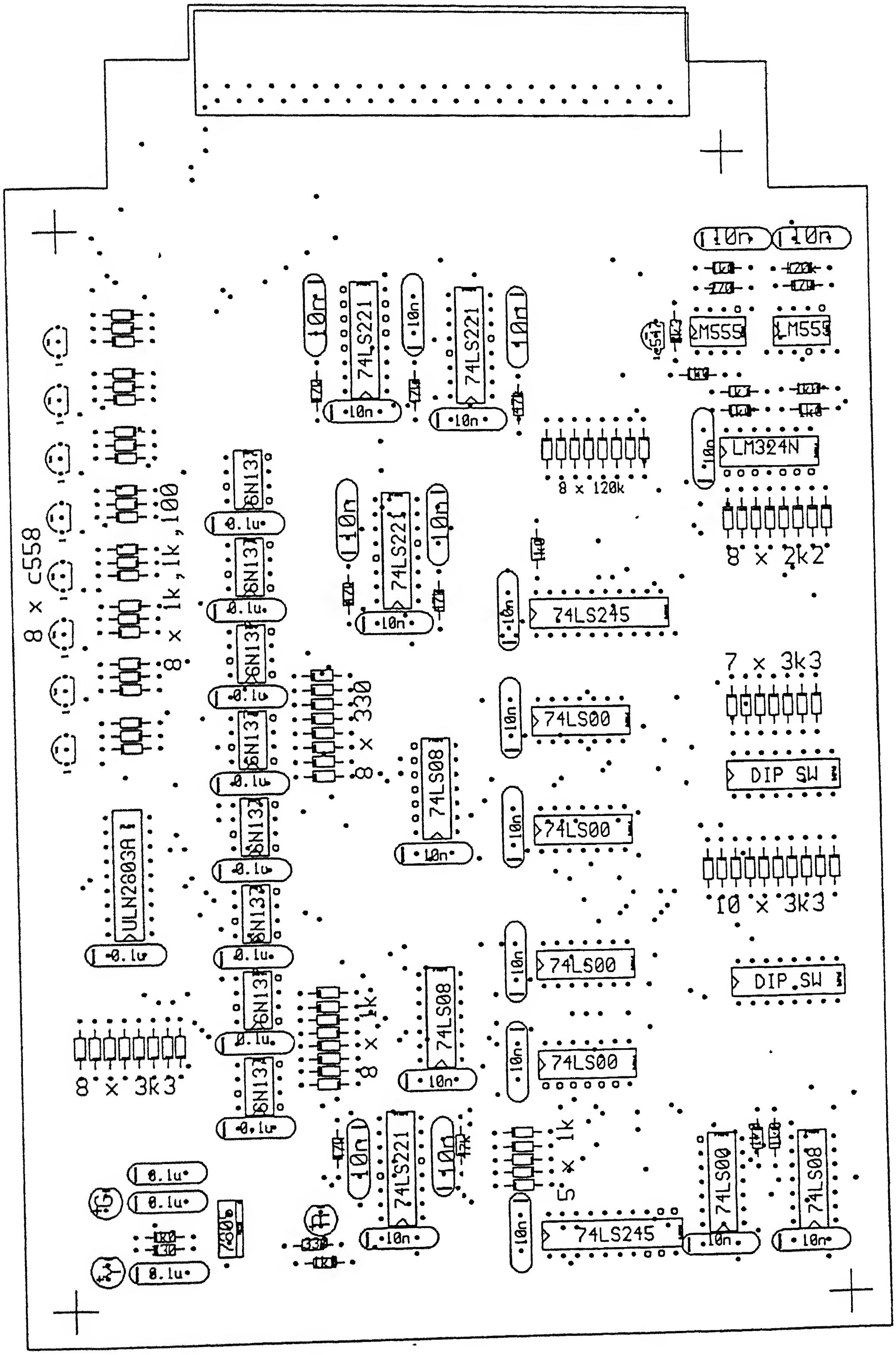

Figure F.1: Firing signals interface card layout.

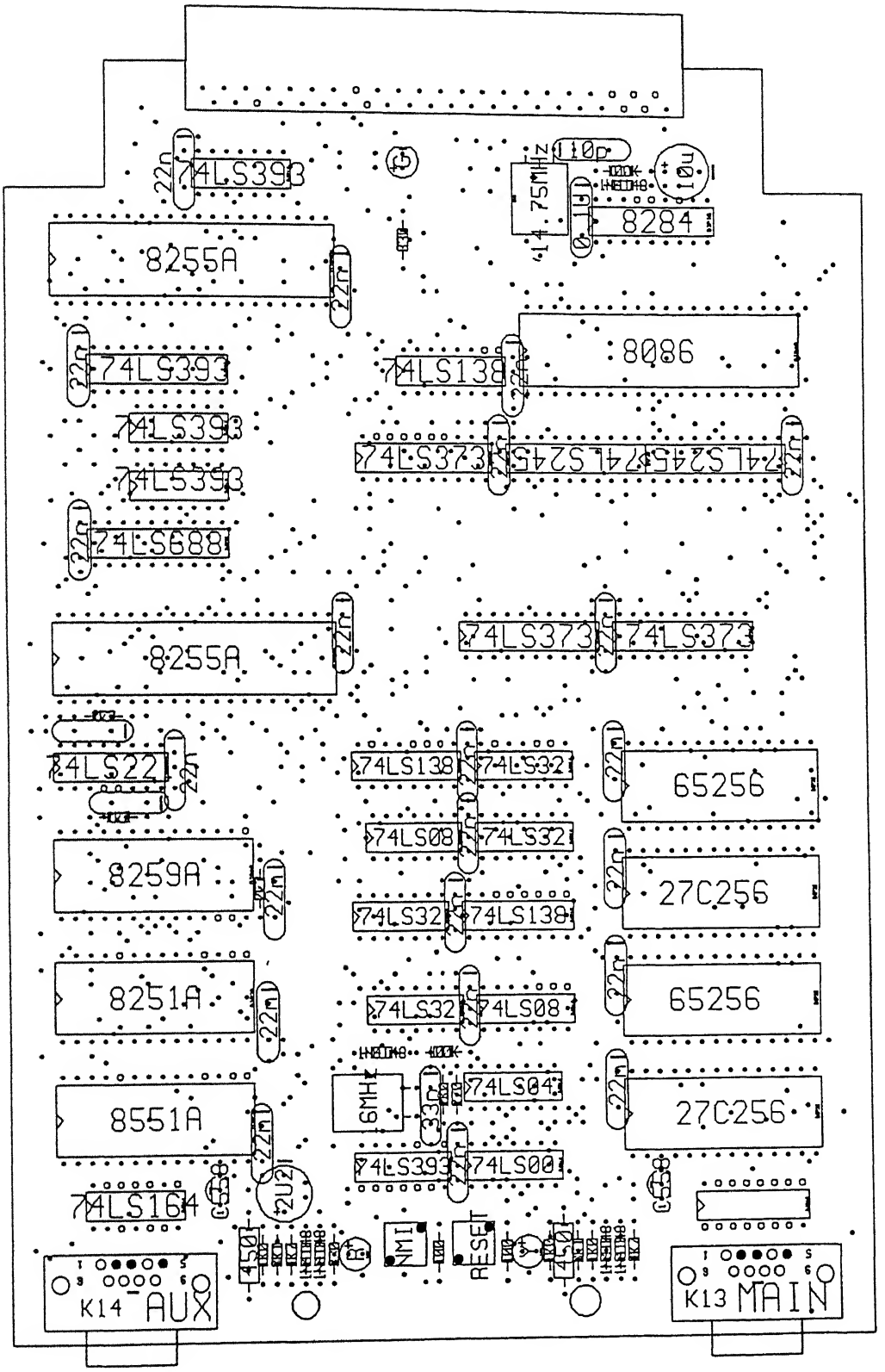

Figure F.2: Controller card layout.

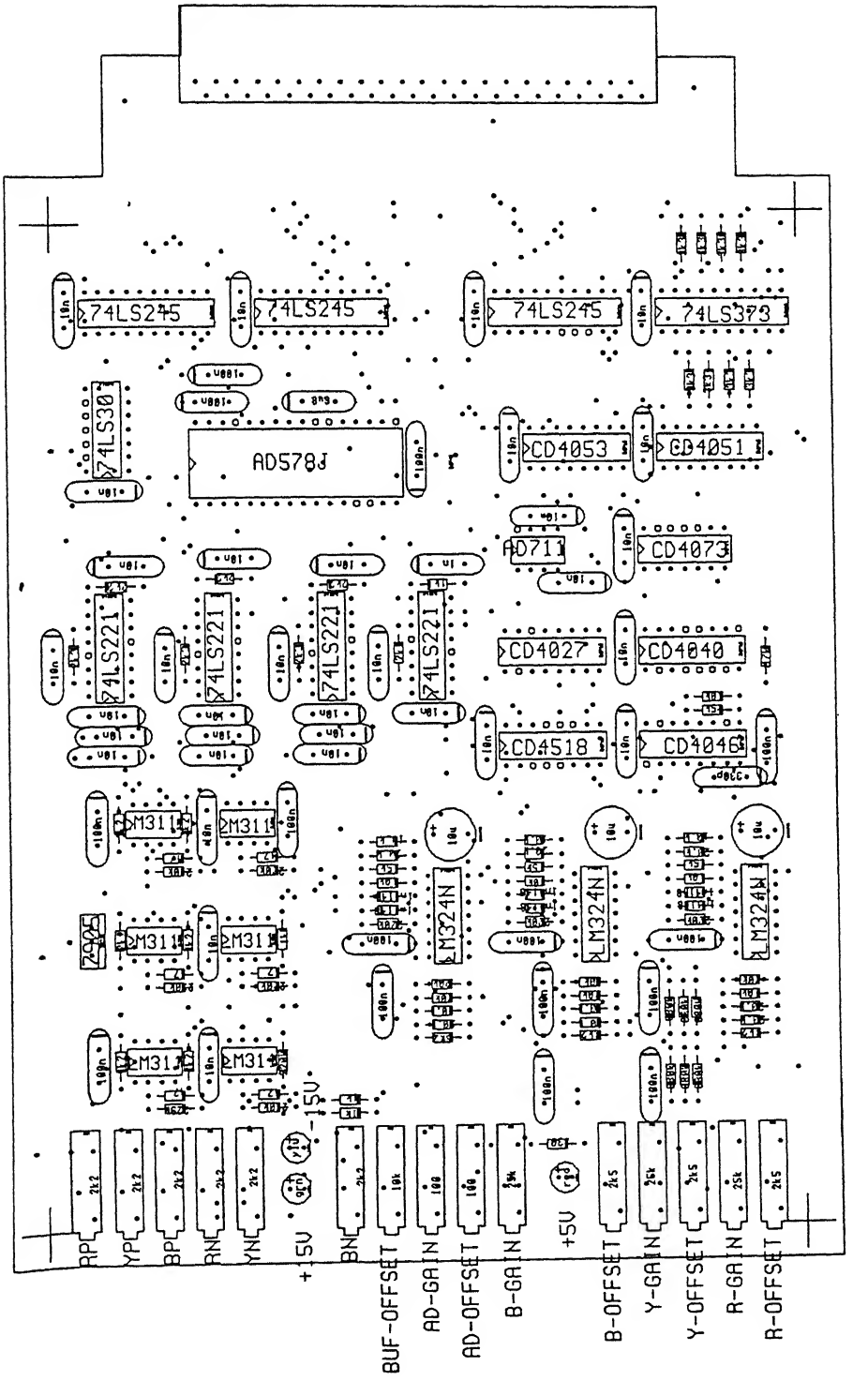

Figure F.3: Analog signal processing card layout.

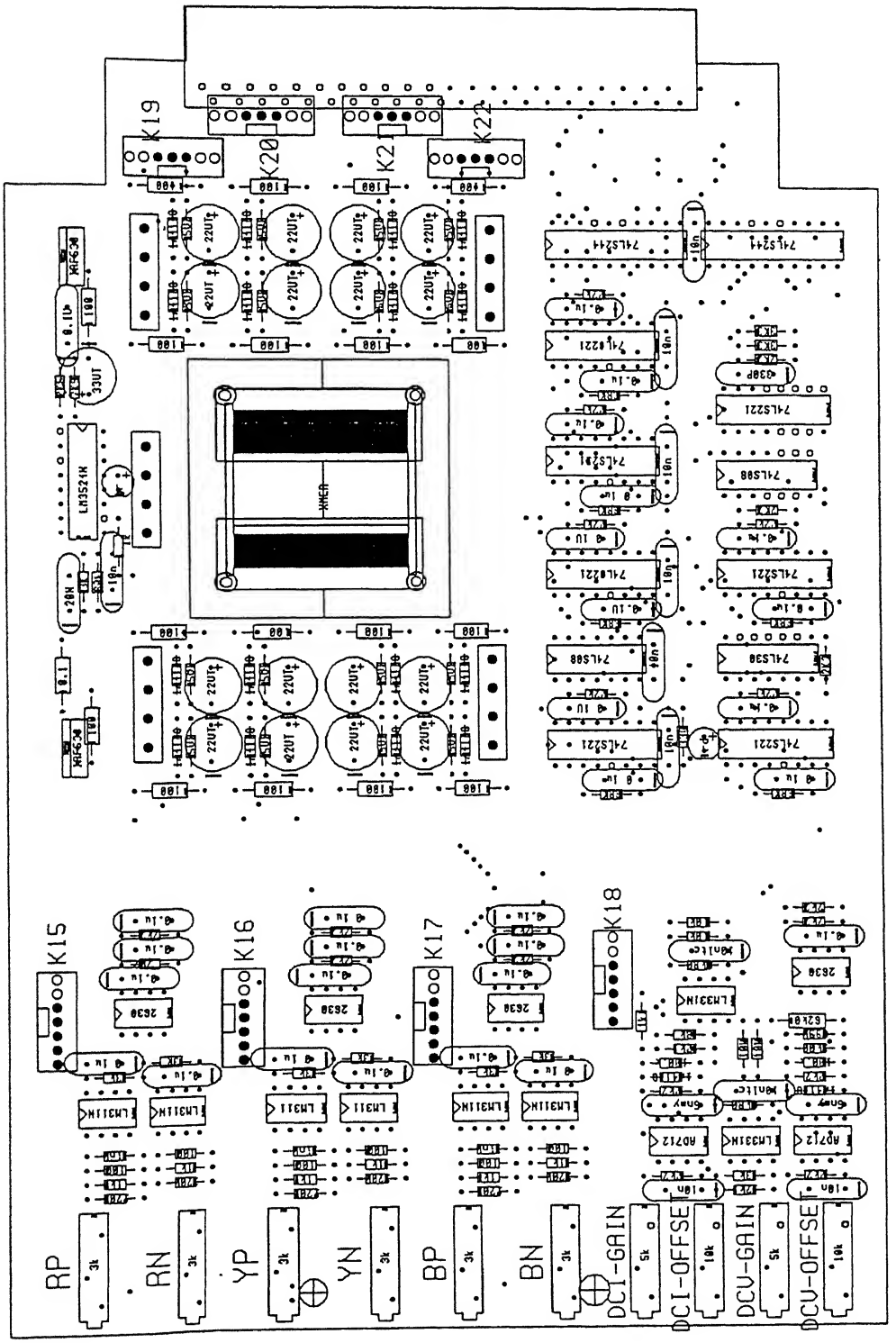

Figure F.4: Live signals interface card layout.

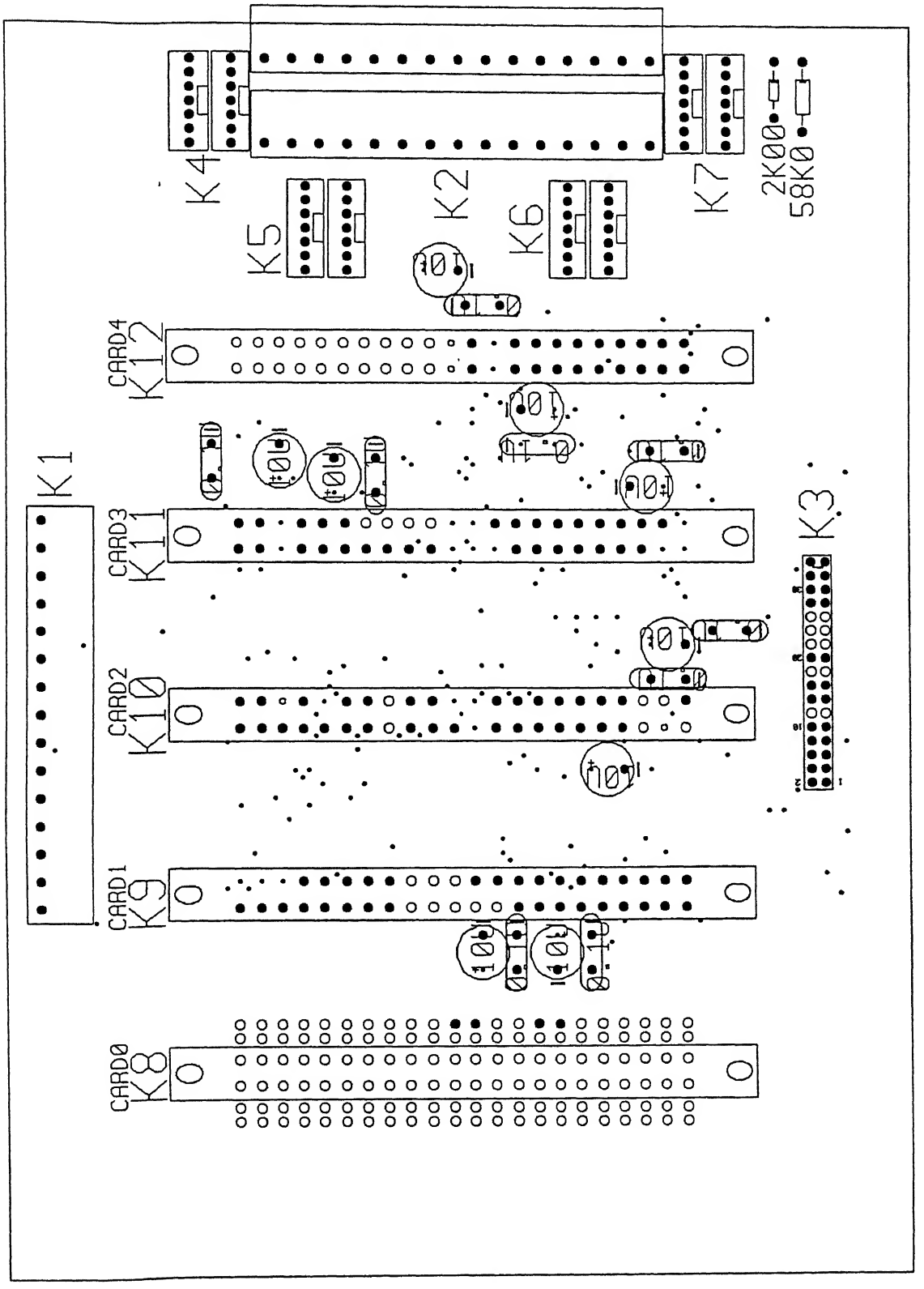

Figure F.5: Mother board layout.